

Compal Confidential
Model Name: VIUS6
File Name: LA-A171P

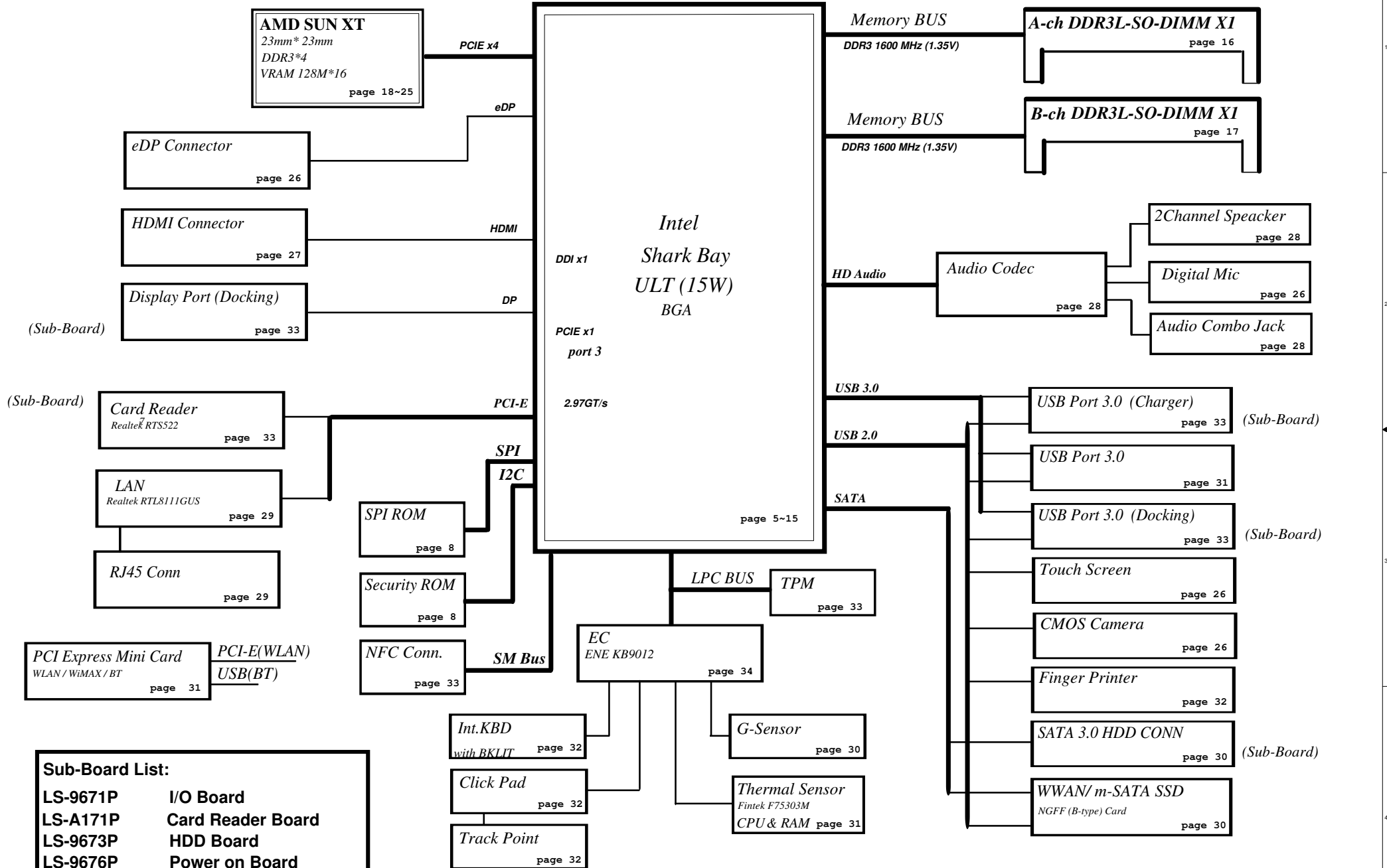
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Guinness-2 M/B Schematics Document

Intel Shark Bay ULT Processor with DDR3L
+AMD SUN XT S3 GPU

REV:1.0_Final

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/02/20	Deciphered Date	2012/07/01	Title	SHEMATIC. MB AA171
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Voltage Rails

power plane State	B+	+5VALW +3VALW	+1.35V	+5VS +3VS +1.5VS +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.675VS +1.05VS	+3VM +1.05VM (SBA Only)
S0	O	O	O	O	O M3 Supported
S3	O	O	O	X	O M3 Supported
S5 S4/AC	O	O	X	X	O M3 Supported
S5 S4/ Battery only	X	X	X	X	
S5 S4/AC & Battery don't exist	X	X	X	X	

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H
Charger	0001 011X b	12H

EC SM Bus2 address

Device	Address	HEX
Thermal Fintek F75303M	1001 101X b	9AH
Thermal ON-semi ADM1032	0100 110X b	4CH
Sinaptics Inter Touch Click Pad	0010 110X b	2CH

PCH SM Bus address

Device	Address	HEX
DDR DIMM1	1001 000X b	A0H
DDR DIMM2	1001 000X b	A4H
Securify ROM	1010 100X b	A8H

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

USB 2.0 Port Table

USB 2.0	Port	3 External USB Port
	0	USB 3.0 Port (I/O Board)
	1	USB 3.0 Port (MB)
	2	USB 3.0 Port (Docking)
	3	Mini Card (WLAN/BT)
	4	Touch Screen
	5	Camera
	6	FPR
	7	WWAN

BOM Structure Table

BTO Item	BOM Structure
Connector	ME@
Unpop	@
AMD GPU	DIS@
Intel UMA	UMA@
MARS GPU	MARS@
TPM	TPM@
SIM	SIM@
SBA	SBA@
Non-SBA	NOSBA@
LAN Switching mode	SWR@
LAN LDO mode	LDO@
VRAM Option	X76@
Samsung VRAM	X76S@
Micron VRAM	X76M@
AOAC Mount	AOAC@
EMI un-Mount	@EMI@
EMI Mount	EMI@

Either SBA@ or NOSBA@

Either SWR@ or LDO@

Either X76S@ or X76M@

USB 3.0 Port Table

Port	
1	USB 3.0 Port (I/O Board)
2	USB 3.0 Port (MB)
3	USB 3.0 Port (Docking)
4	

PCIE Port Table

Port	Lane	
1		LAN WLAN Cardreader
2		
3		
4		
5	0	GPU
	1	
	2	
	3	
6	0	
	1	
	2	
	3	

SATA Port Table

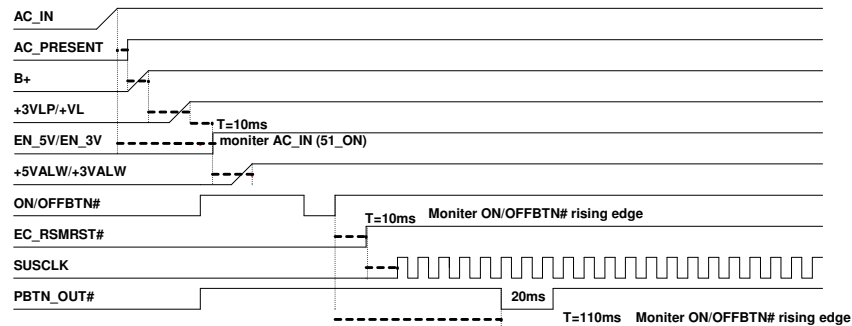
Port	
3	
2	
1	NGFF SSD
0	HDD

CPU

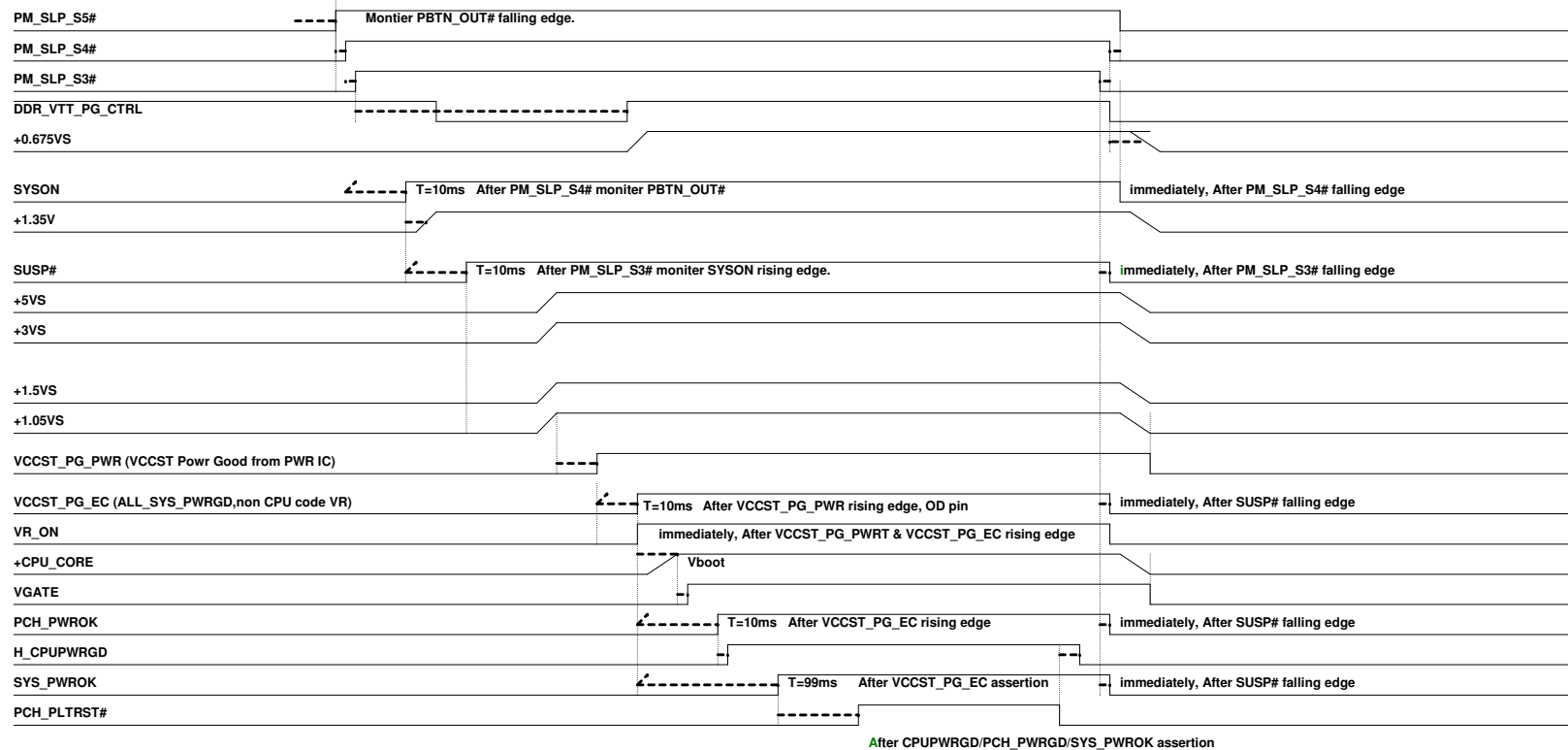
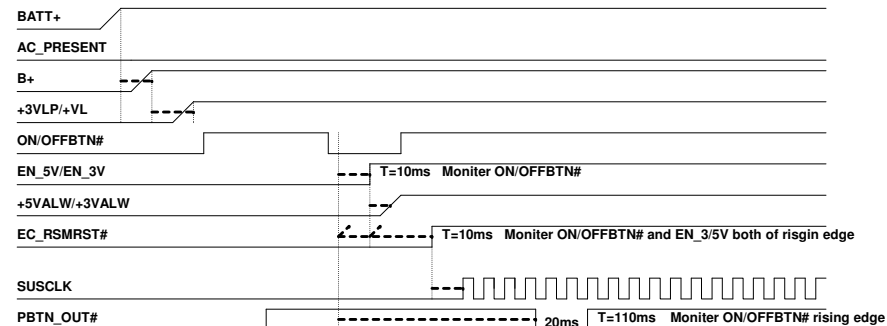
U1 Haswell ULT 2+2 0.8GHz CPU1@ SA000067010	U1 Haswell ULT 2+2 1.2GHz CPU2@ SA00006G190	U1 Haswell ULT 2+3 0.2GHz CPU3@ SA000067H20	U1 Haswell ULT 1.5GHz CPU4@ SA00006SJ20	U1 Haswell ULT 1.4GHz CPU5@ SA00006ST30	PCB ZZZ LA-A171P DA PCB DA20YW00100
U1 Haswell ULT 1.6GHz CPU6@ SA00006SM40	U1 Haswell ULT 1.7GHz CPU7@ SA00006SX40	U1 Haswell ULT 1.8GHz CPU8@ SA00006SL50	U1 Haswell ULT 1.3GHz CPU9@ SA00006NM30	U1 Haswell ULT 1.7GHz C0 CPU10@ SA00006SS20	VRAM ZZZ2 MICRON_512MB X76M@ X7646039L01
U1 Haswell ULT 1.7GHz C0 CPU11@ SA00006SX50	U1 Haswell ULT 1.6GHz C0 CPU12@ SA00006SM70	U1 Haswell ULT 1.7GHz C0 CPU13@ SA00006SL60	U1 Haswell ULT 1.7GHz C0 CPU14@ SA00006SL60	U1 Haswell ULT 1.7GHz C0 CPU15@ SA00006SS60	ZZZ1 Samsung_512MB X76S@ X7646039L02

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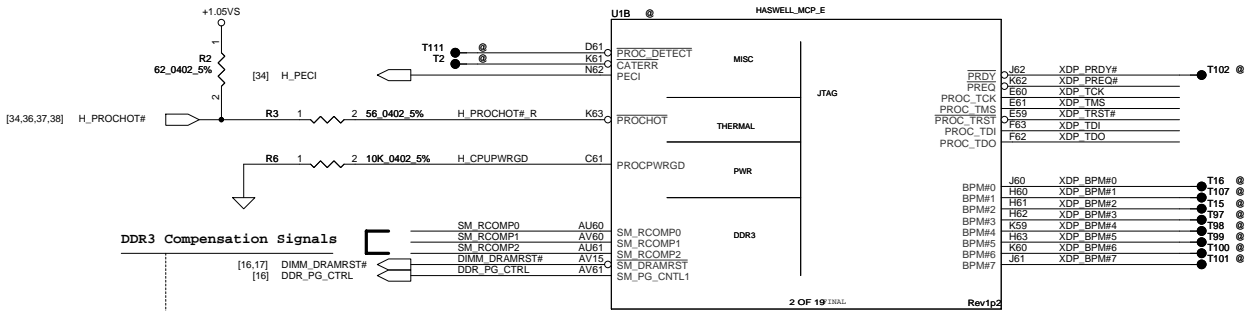
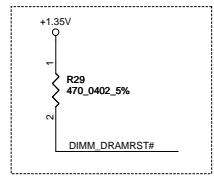
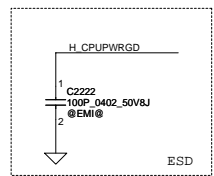
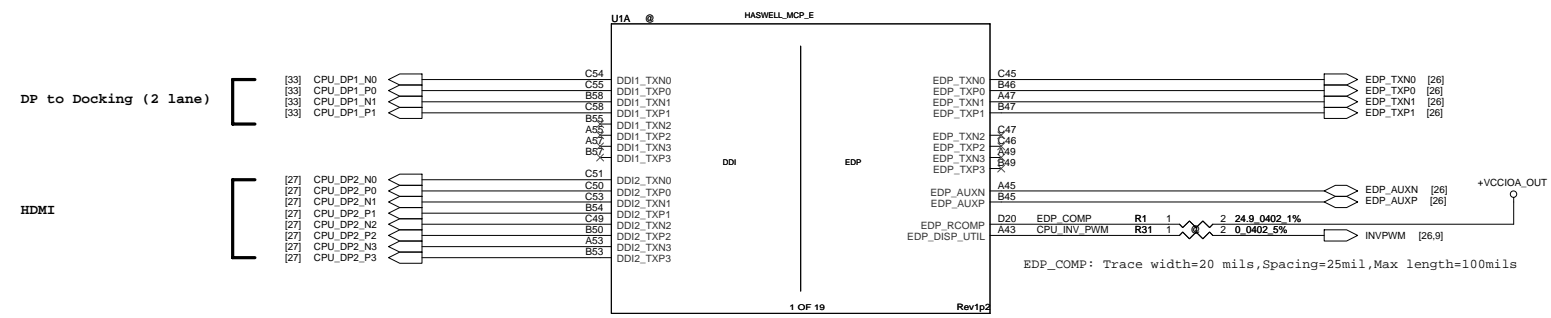
[AC Mode]



[DC Mode]

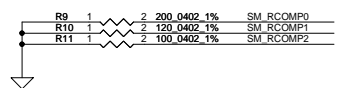


DDI/ MSIC/ XDP

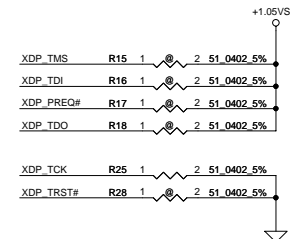


DDR3 Compensation Signals

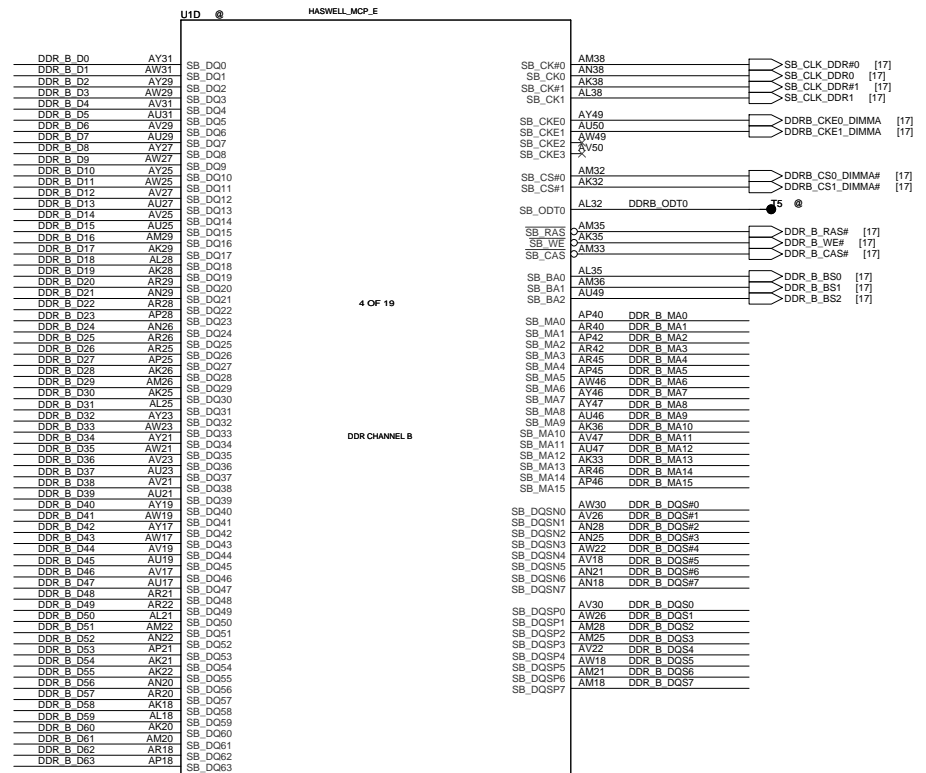
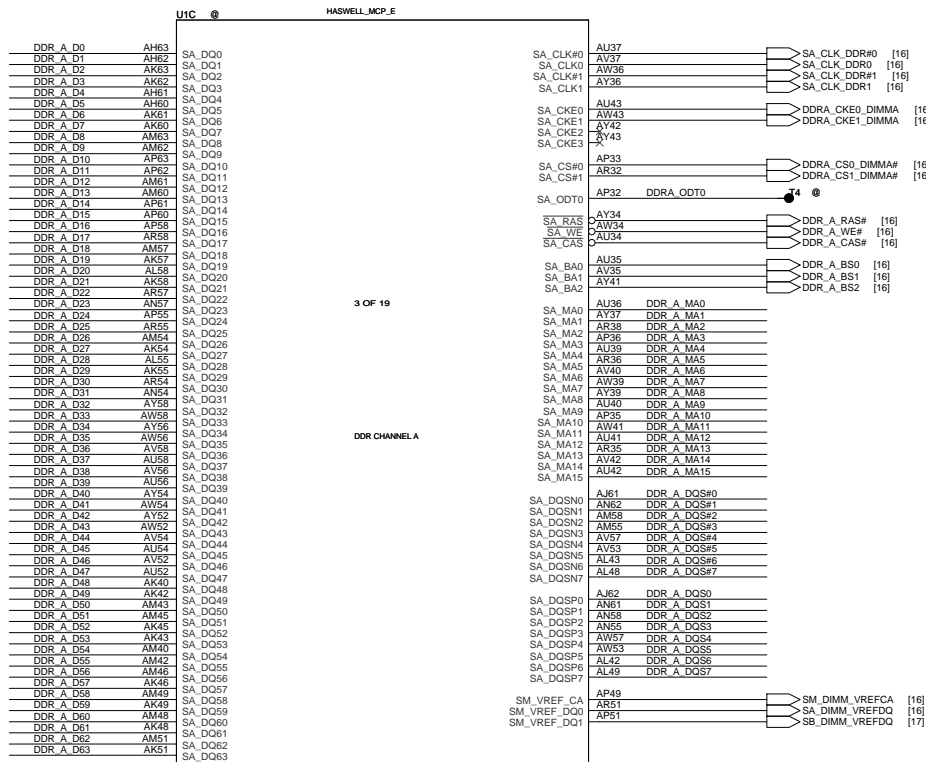
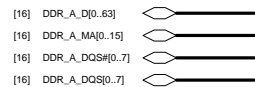
DDR3 Compensation Signals:
20 mils to comp signals
25 mils to non-comp signals
500 mil for Max trace length



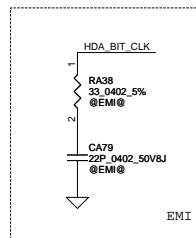
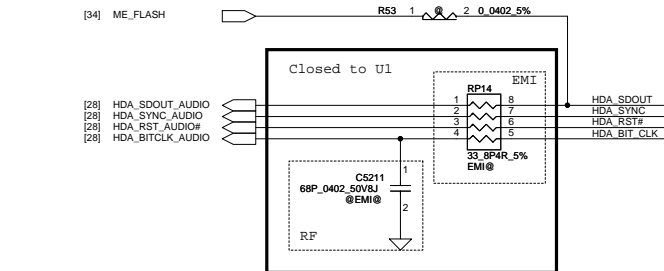
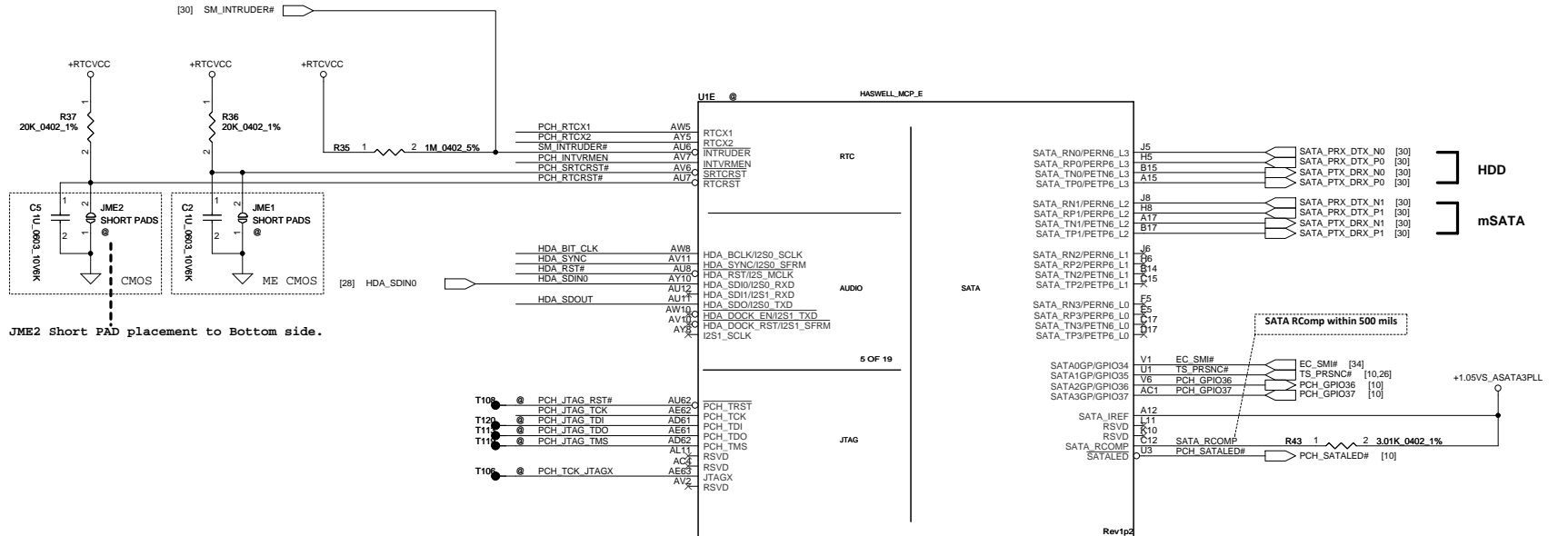
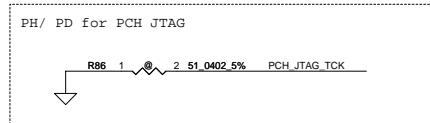
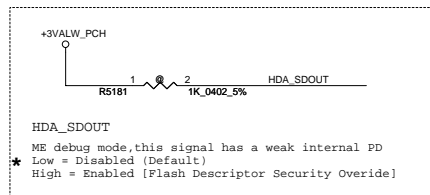
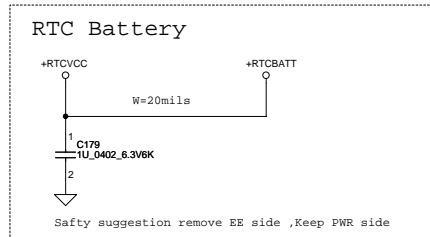
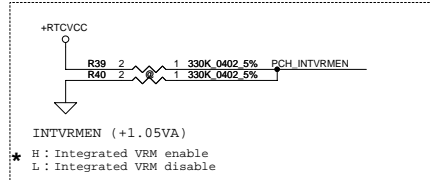
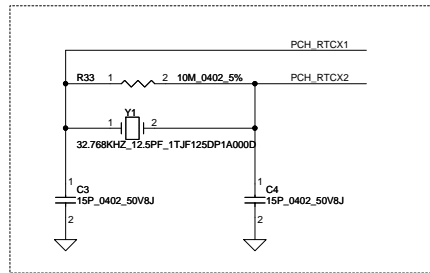
PU/PD for JTAG signals



Memory I/F

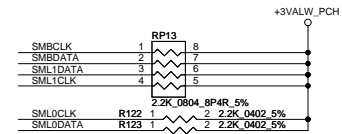
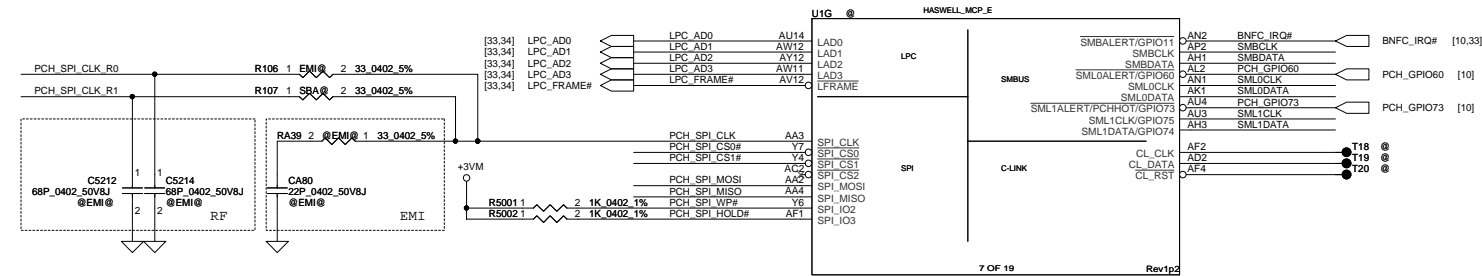
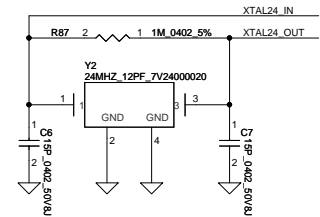
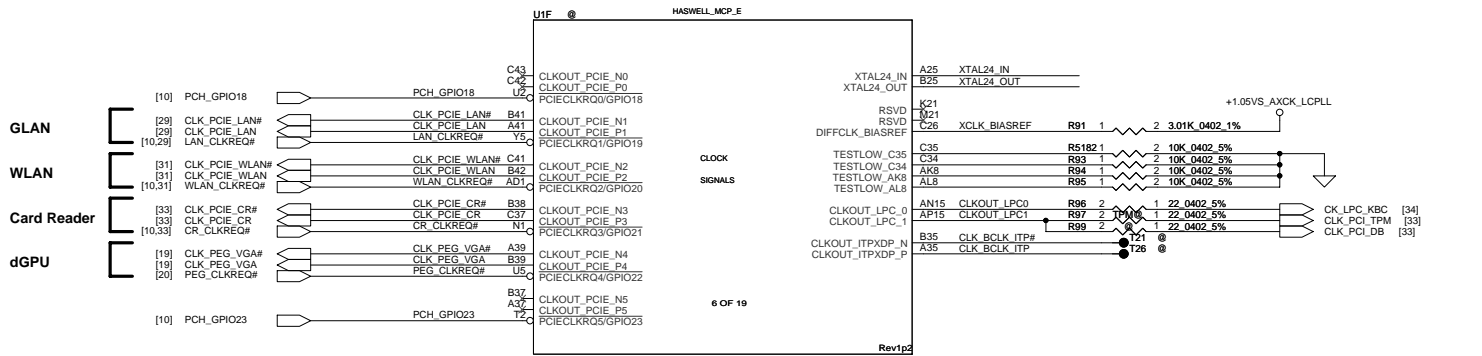


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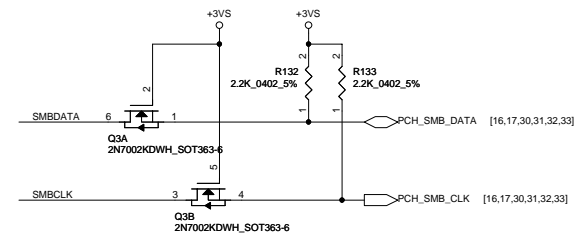


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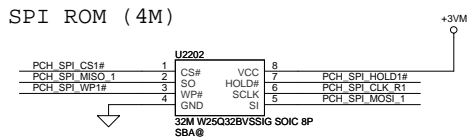
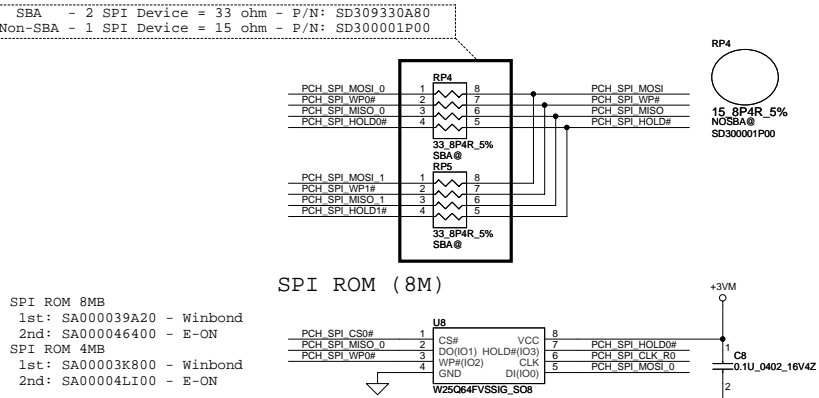
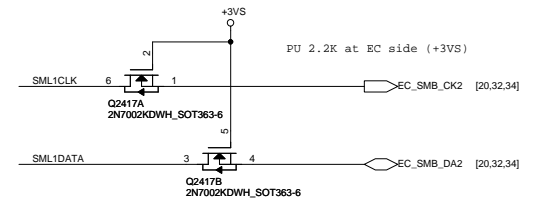
CLK/ SPI/ SMBUS



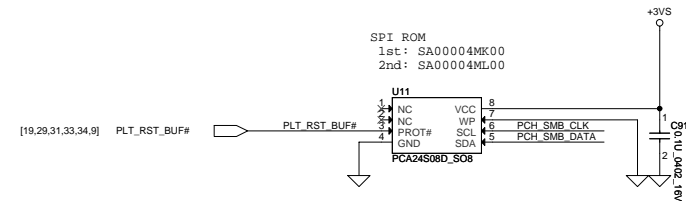
SMBus : SPD/PCIE/Security/TP/NFC



SML1 Bus :EC/Sensors



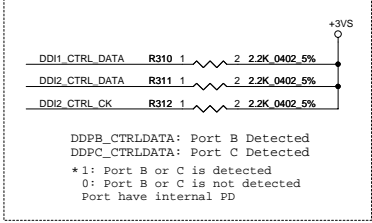
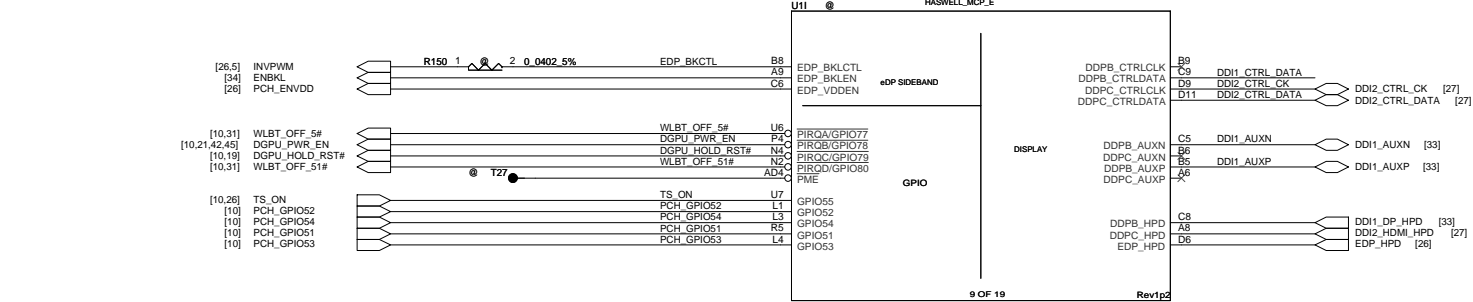
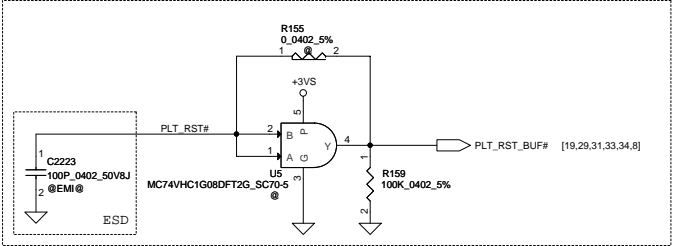
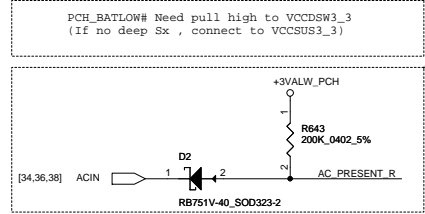
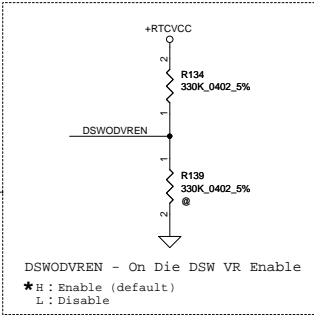
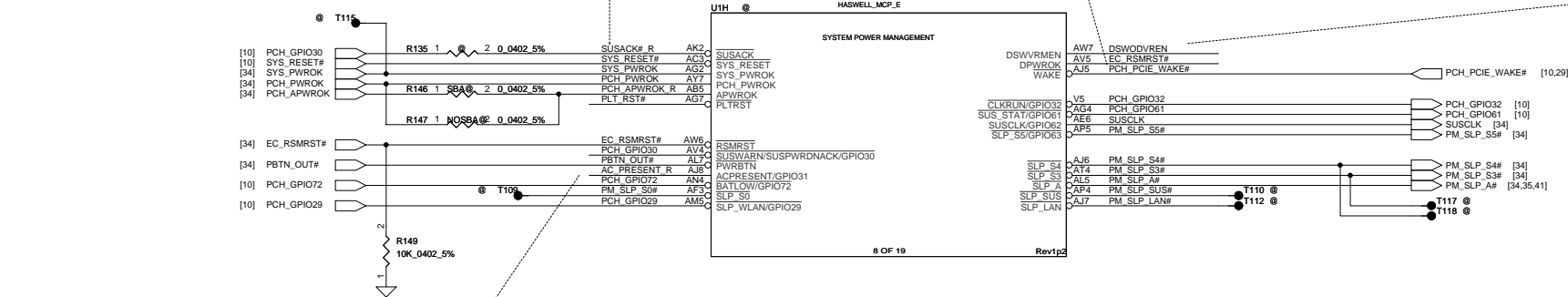
Security ROM



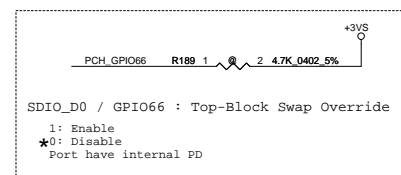
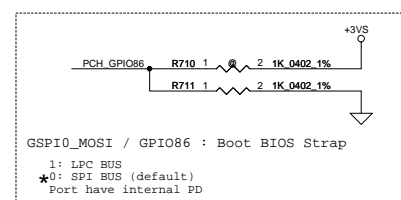
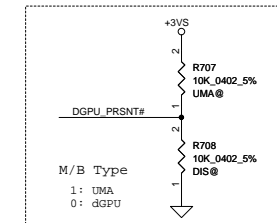
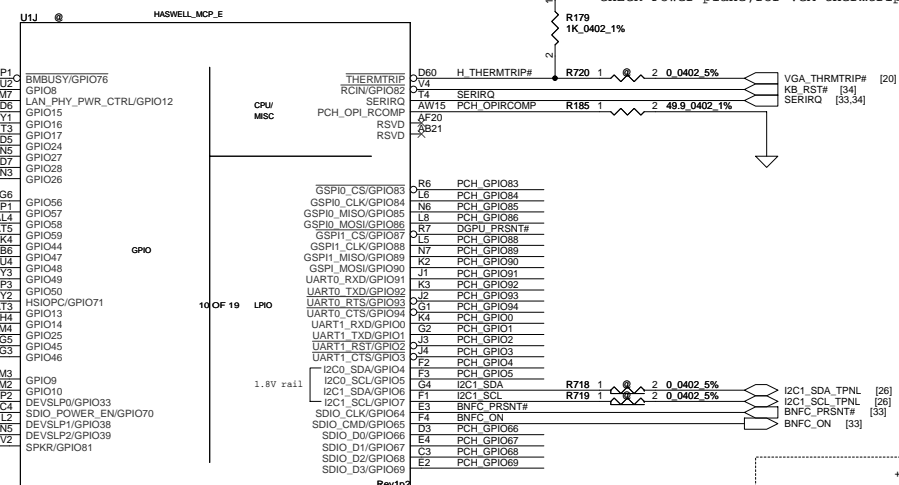
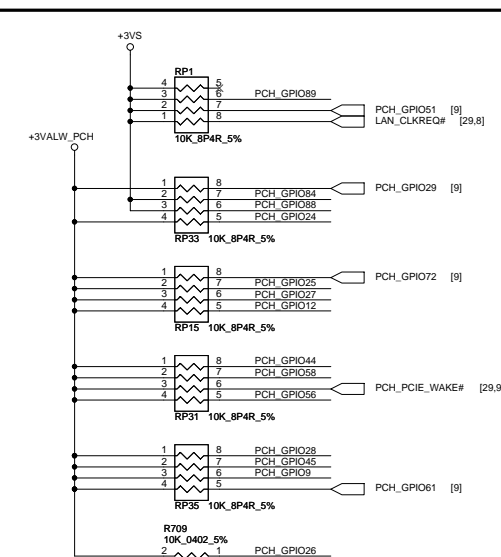
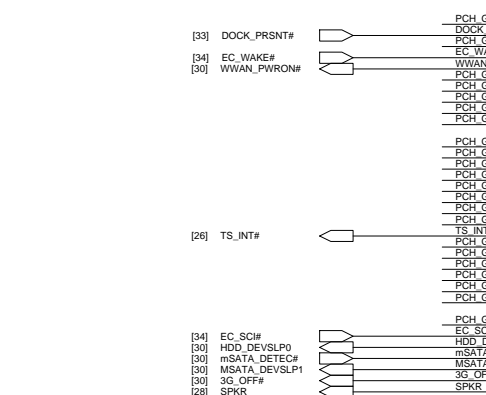
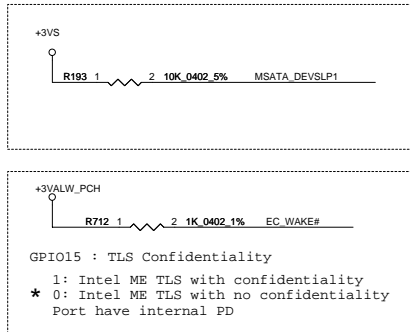
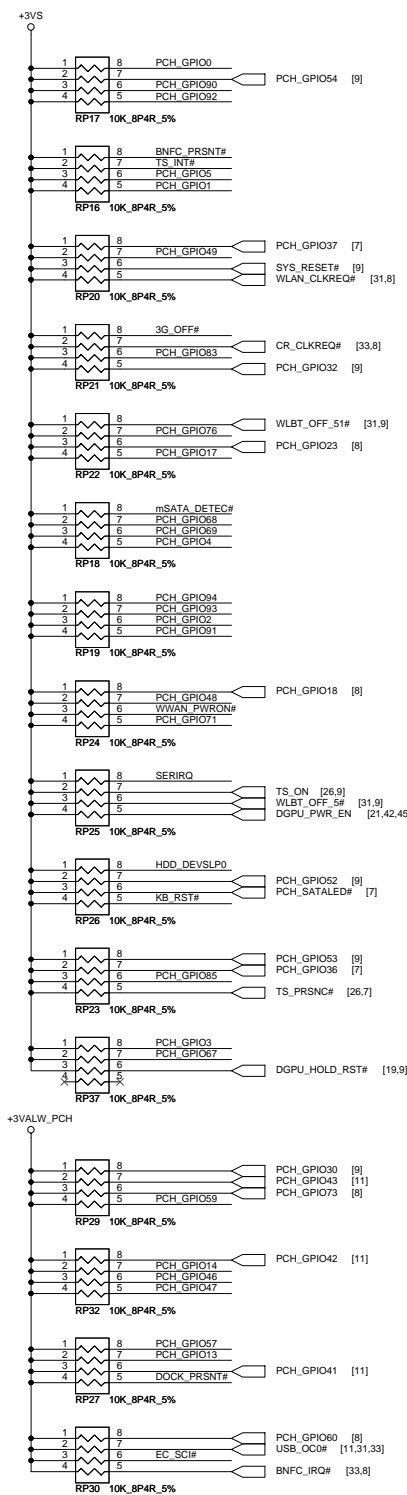
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PM/ GPIO/ DDI

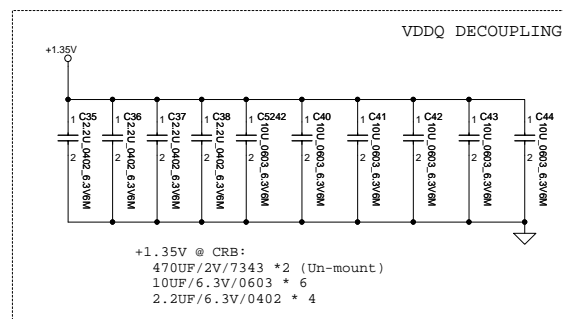
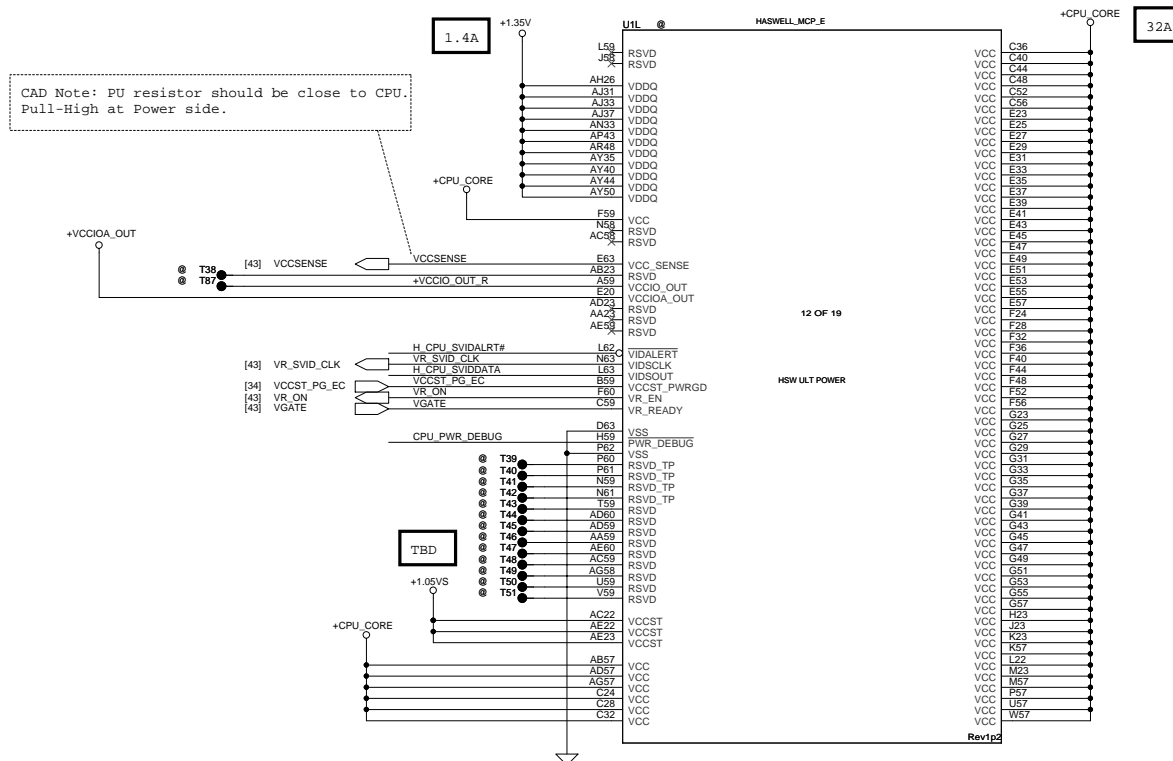
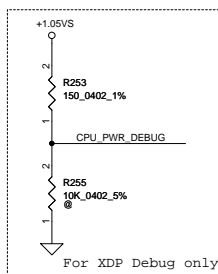
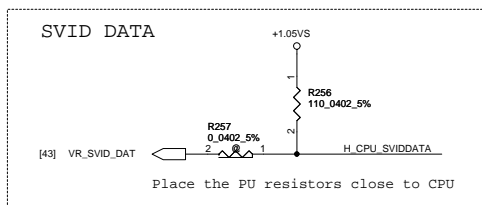
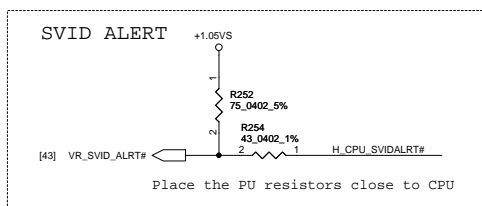
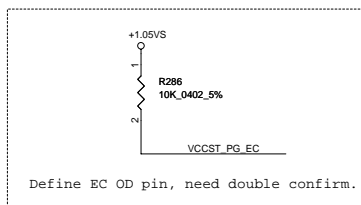
Note: SUSACK# and SUSWARN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit.
CAN be NC ,if not support Deep Sx



GPIO/ LPIO



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					HSW MCP(6/11) GPIO,LPIO		
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					Date:		Friday, February 28, 2014



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					HSW MCP(8/11) Power		
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Power

41mA

42mA

57mA

200mA

31mA

1838mA

63/62mA

18mA

658mA

1741/1632mA

41mA

3mA

17mA

Only available on External Suspend VR powered.

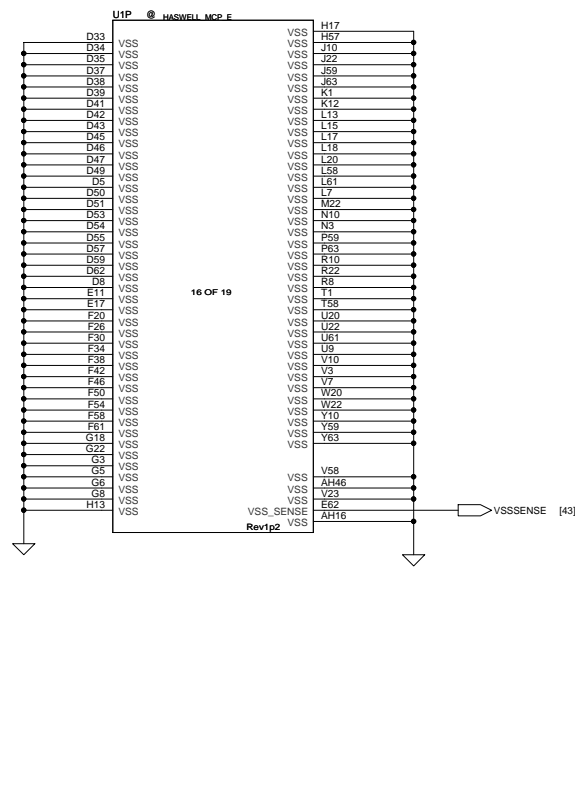
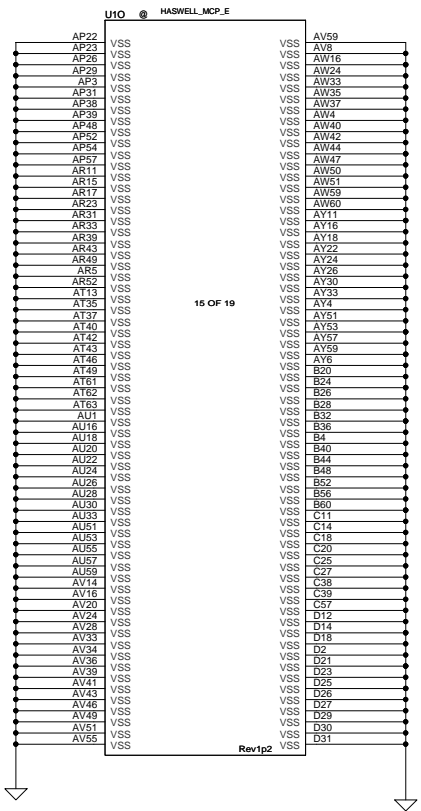
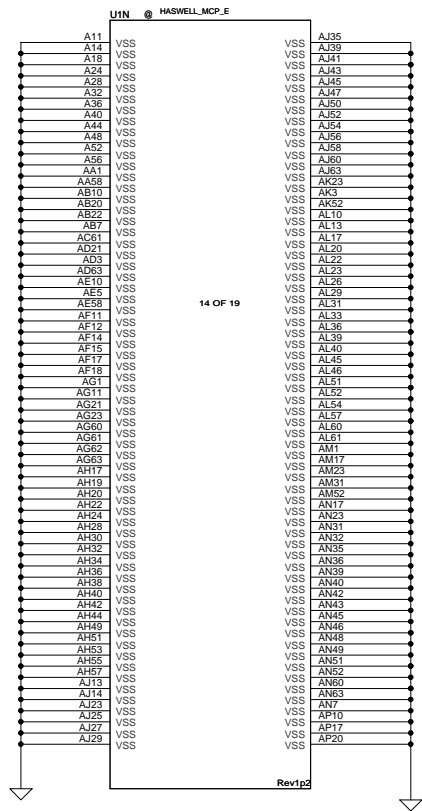
DcpSus1= 109mA

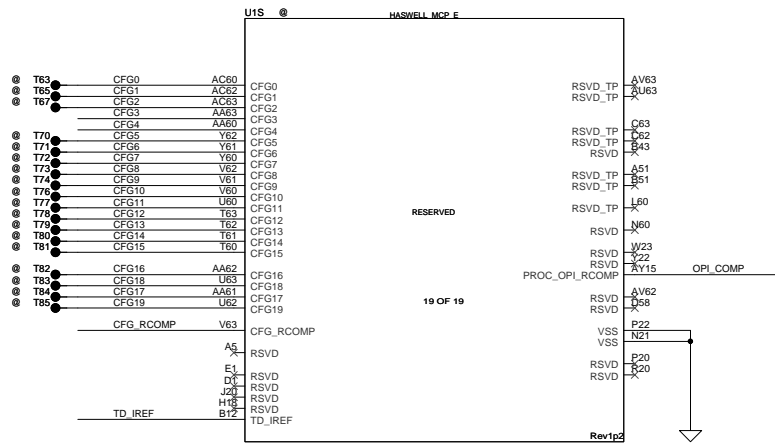
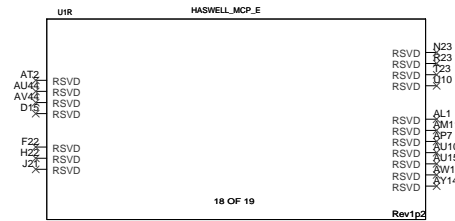
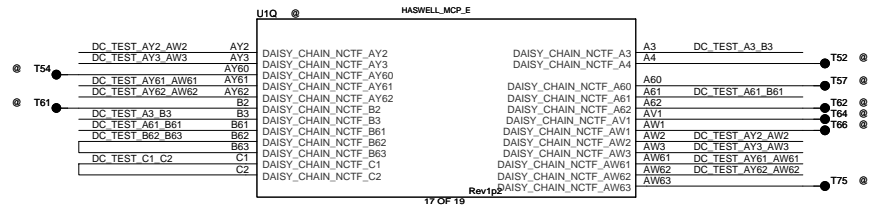
DcpSus2= 25mA

DcpSus3= 10mA

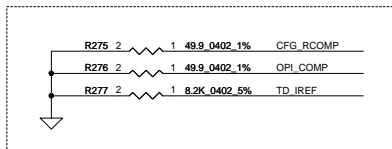
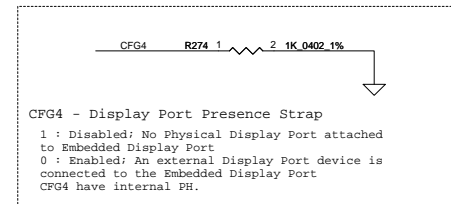
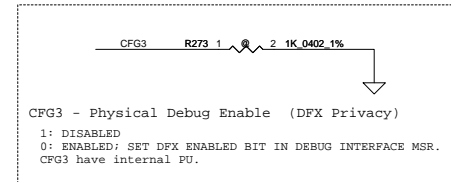
DcpSus4= 1mA

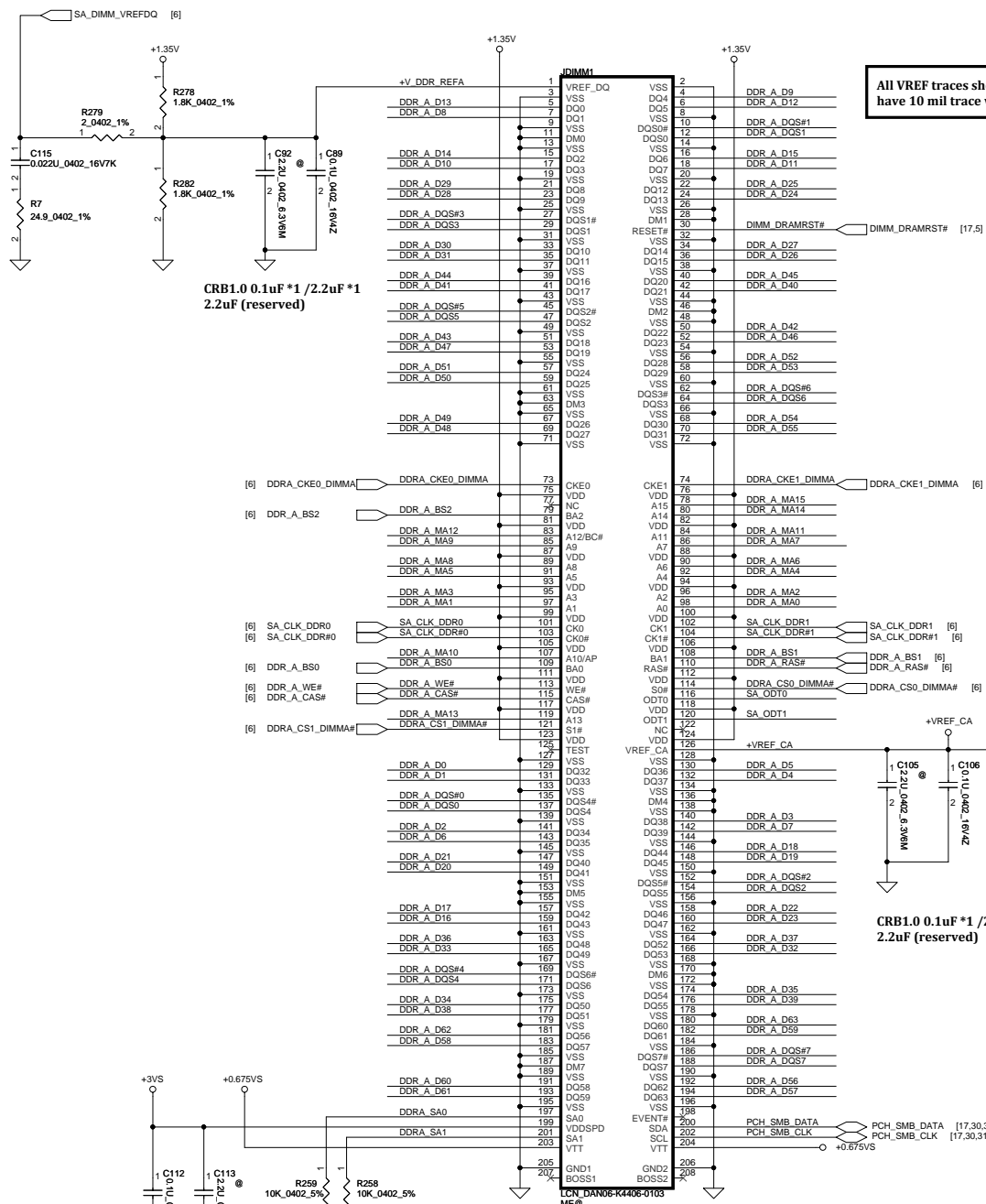
Security Classification	Compal Secret Data		Title	
Issued Date	2013/02/20	Deciphered Date	2012/07/01	HSW MCP(9/11) Power
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Size	Custom	Document Number	40190J	Rev D
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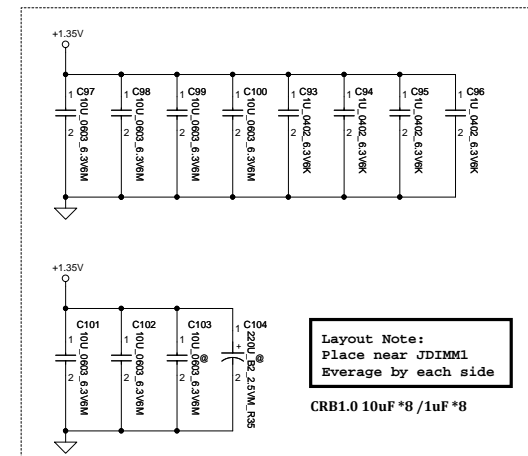


CFG Straps for Processor



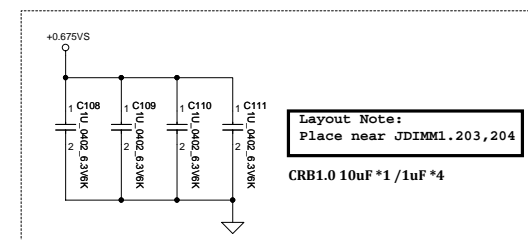
DIMM A

All VREF traces should have 10 mil trace width



Layout Note:
Place near JDIMM1
Everage by each side

CRB1.0 10uF *8 /1uF *8



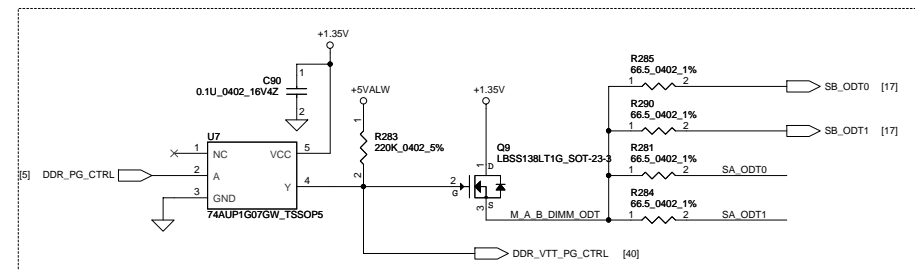
Layout Note:
Place near JDIMM1.203,204

CRB1.0 10uF *1 /1uF *4

CHANNEL A /TYPE :Reverse / H:4mm

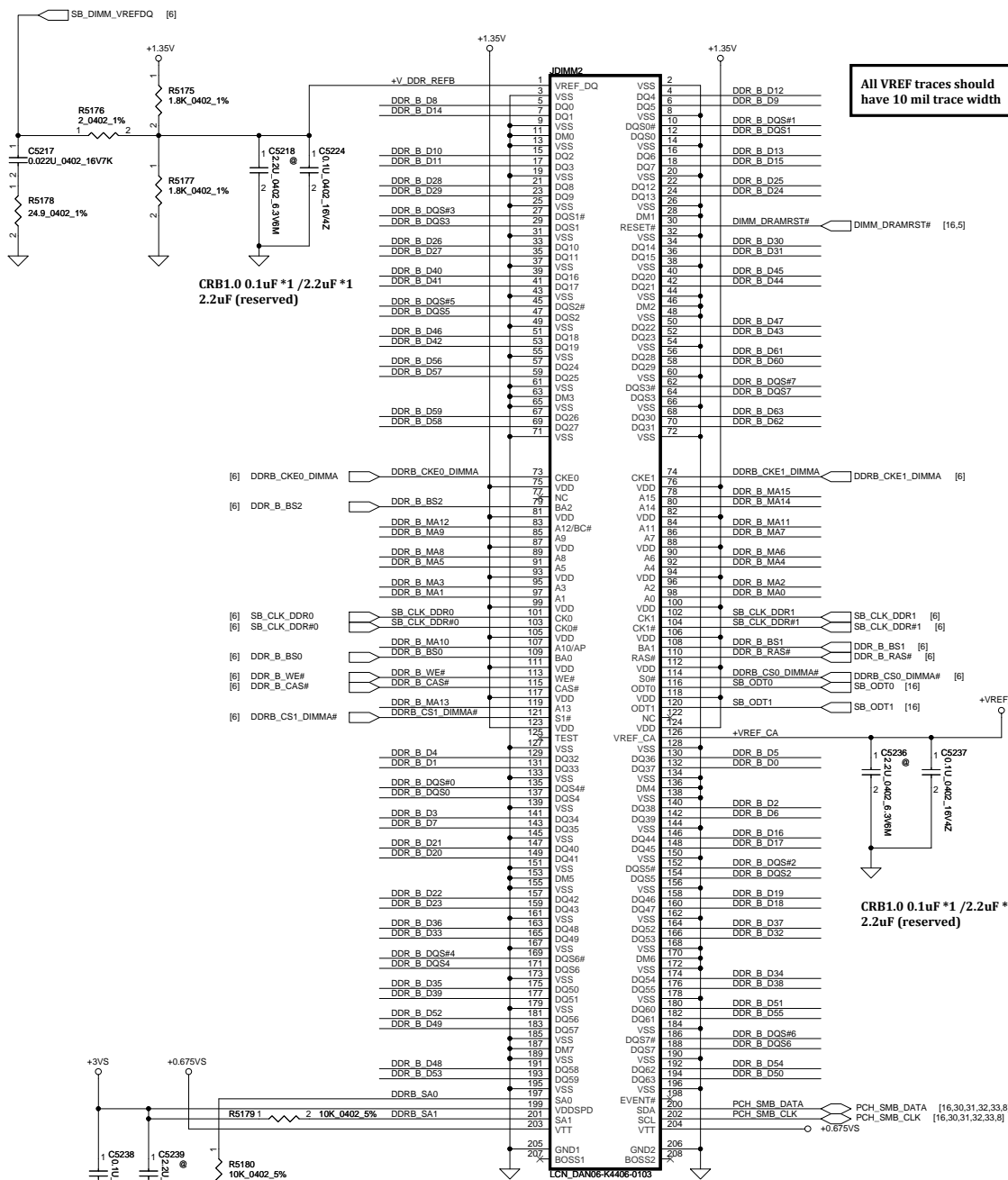
```
CHA SPD ADDRESS IS 0xA0
CHA TS ADDRESS IS 0x30
```

P/N:SP07000LT00



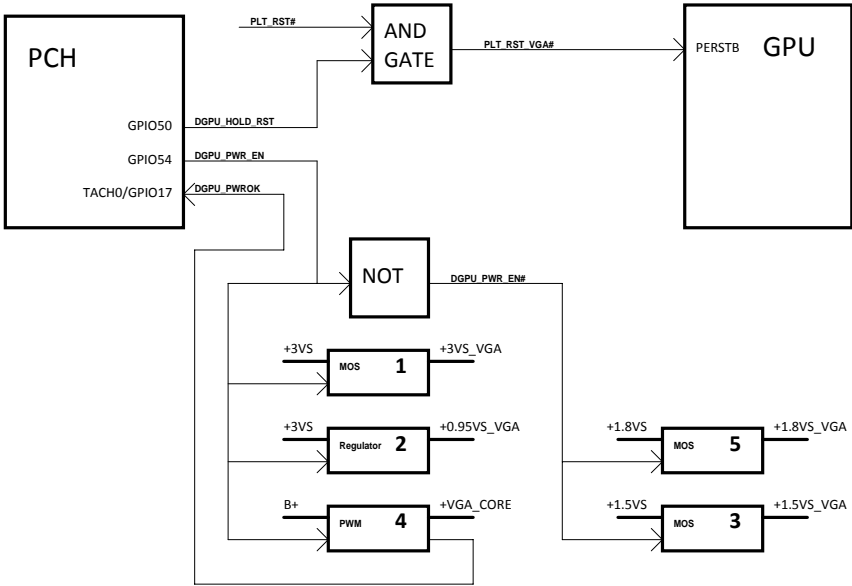
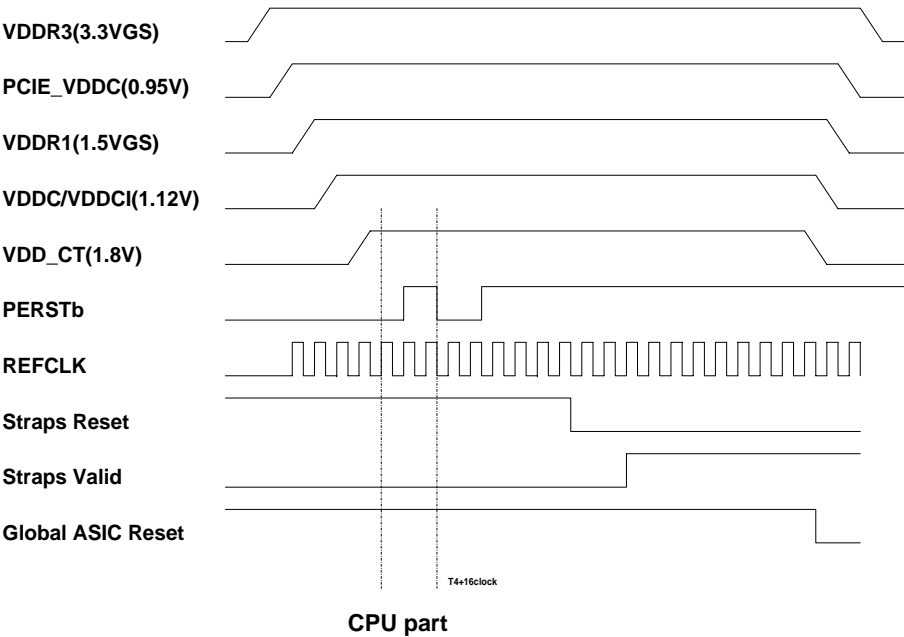
Security Classification	Compal Secret Data			Compal Electronics, Inc.			
Issued Date	2013/02/20	Deciphered Date	2012/07/01	Title	DDRIII DIMMA		
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				Date	40190J		
				Friday, February 28, 2014	Sheet 16 of 46		

DIMM B

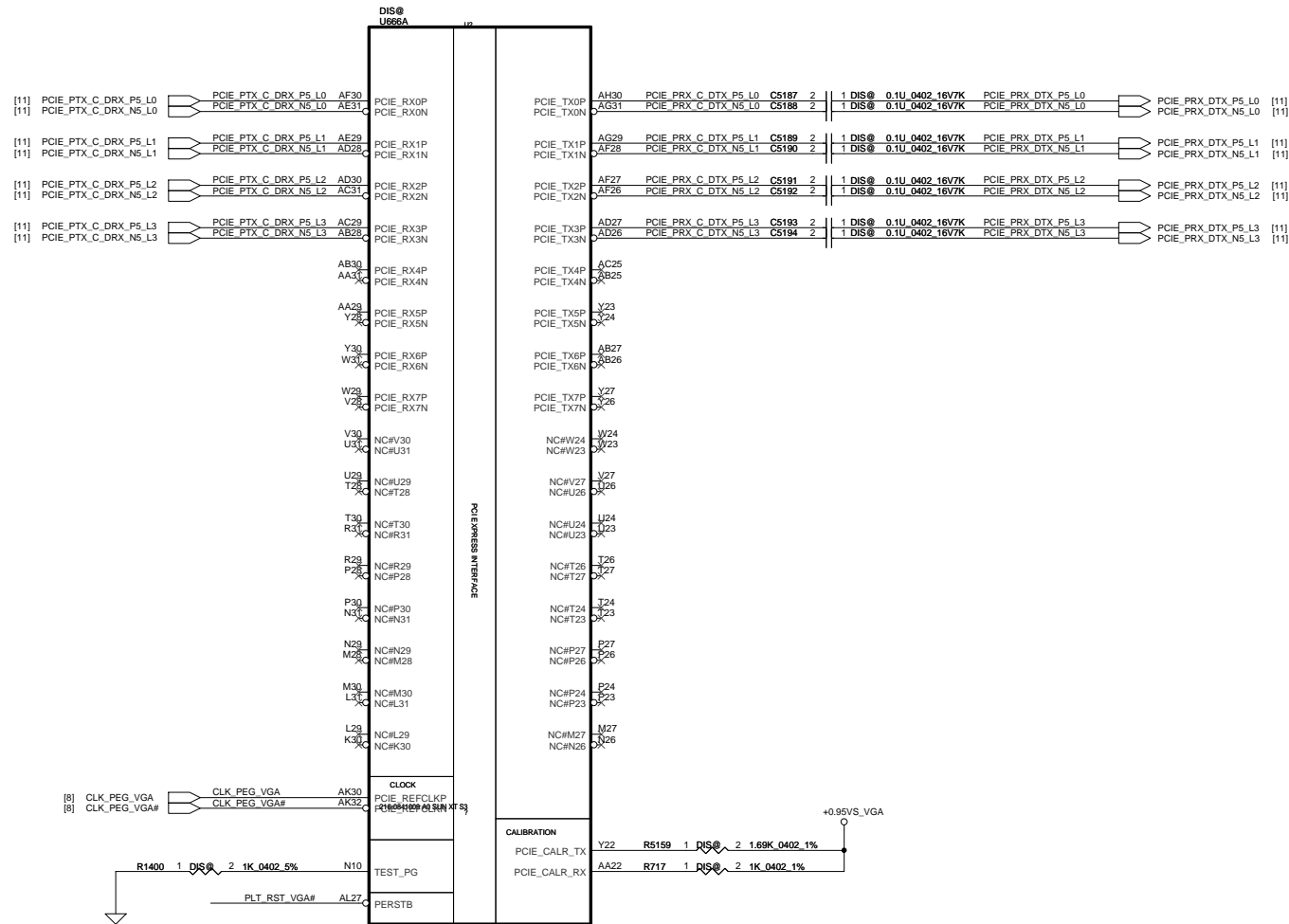


Power-Up/Down Sequence

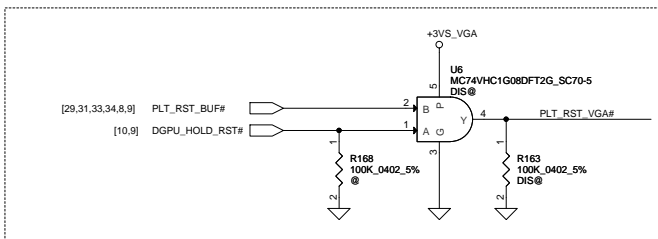
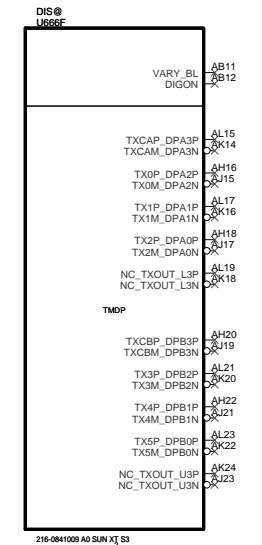
1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
2. The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
3. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
4. For power down, reversing the ramp-up sequence is recommended.



PCIE/ DP

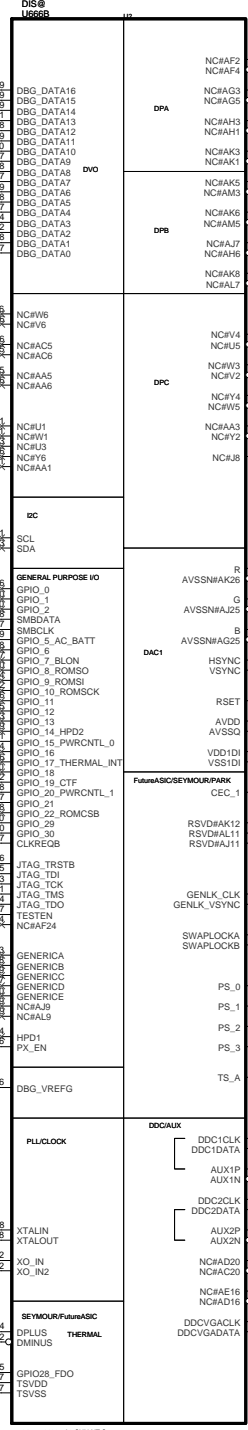
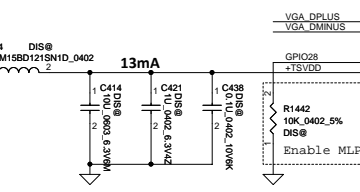
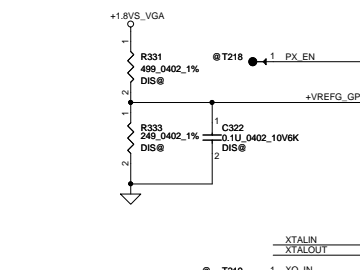
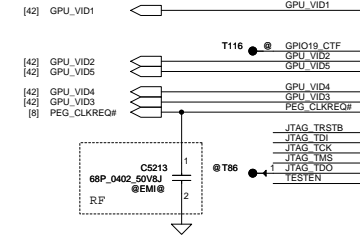
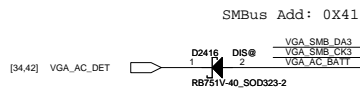
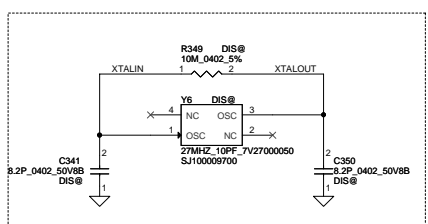
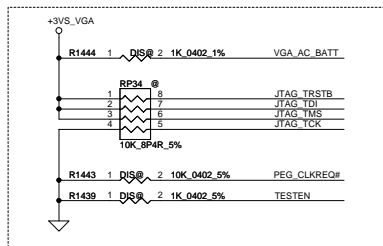
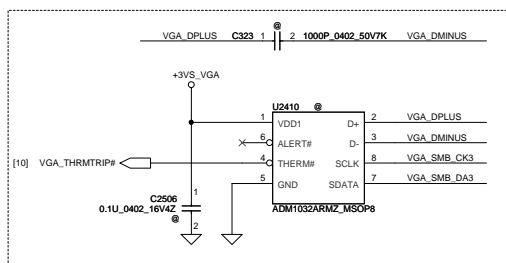
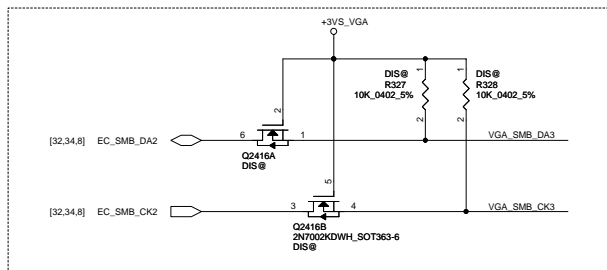


No Use GPU Display Port output



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				Date: Friday, February 28, 2014	Sheet 19 of 46

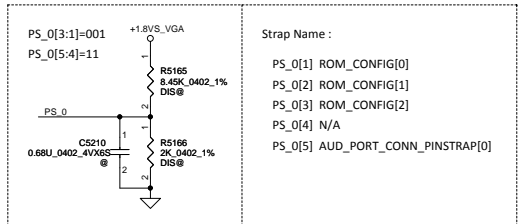
MSIC



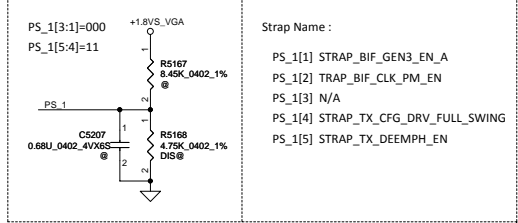
Resistor Divider Lookup Table			
R_pu (ohm)	R_pd (ohm)	Bitd [3:1]	
NC	4.75k	000	
8.45k	2k	001	
4.53k	2k	010	
6.98k	4.99k	011	
4.53k	4.99k	100	
3.24k	5.62k	101	
3.4k	10k	110	
4.75k	NC	111	

0402 1% resistors are required

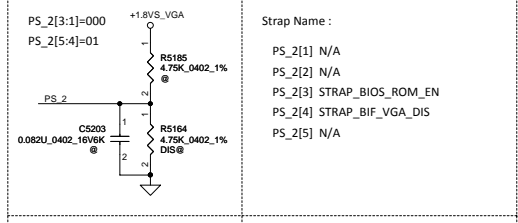
Capacitor Divider Lookup Table	
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11



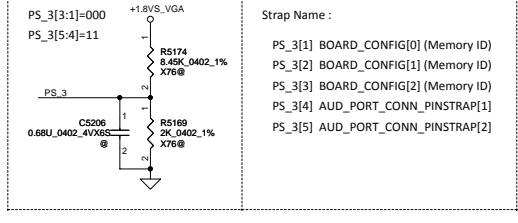
Strap Name :
PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]



Strap Name :
PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN



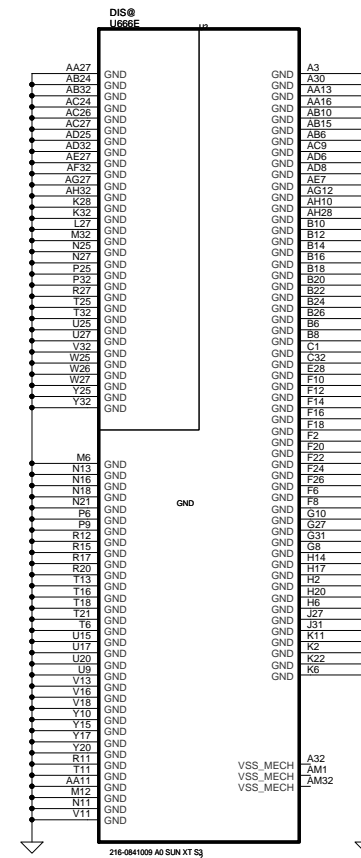
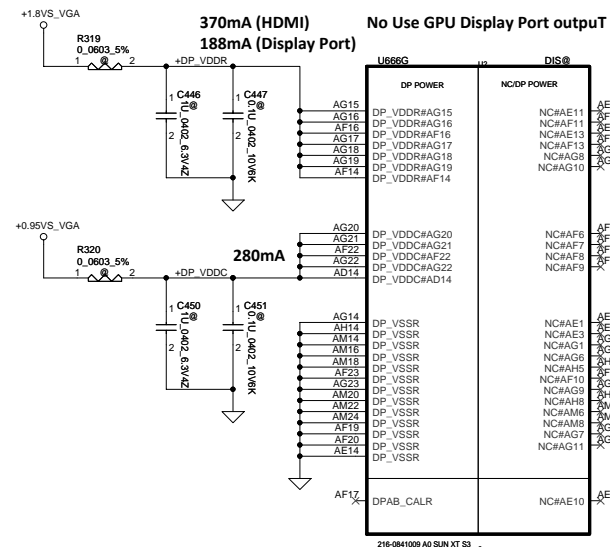
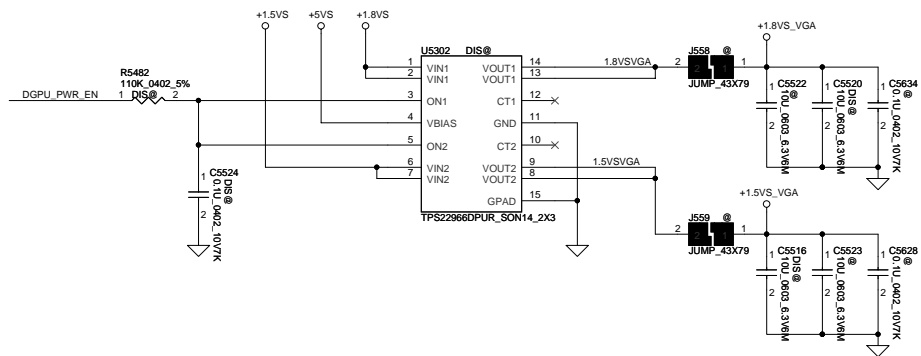
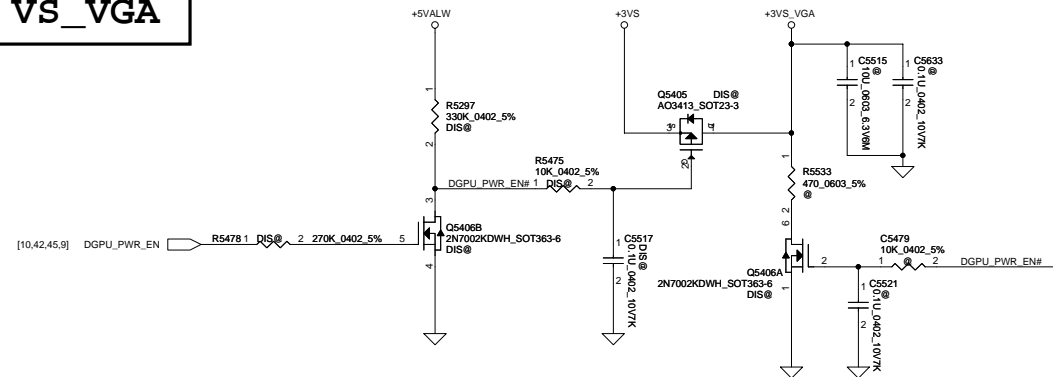
Strap Name :
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A



Strap Name :
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

Memory ID	R_pu (ohm)	R_pd (ohm)	Memory Type	Configuration	Size
PS_3[3..1]	R5174	R5169			
0 0 1	8.45k	2k	gDDR3-2133	Samsung K4W2G1646E-BC1A P/N: SA000068U00	1GB
0 1 0	4.53k	2k	gDDR3-2000	Micron MT41J128M16JT-093G P/N: SA000067500	1GB
0 1 1	6.98k	4.99k	gDDR3-1866	Samsung K4W4G1646B-HC11 P/N: SA000068R00	2GB
1 0 0	4.53k	4.99k	gDDR3-1866	Micron MT41K256M16HA-107G: E P/N: SA000065D00	2GB

VS_VGA



PWR / GND

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				Custom	40190J	D
Date:				Friday, February 28, 2014	Sheet	21 of 46

POWER

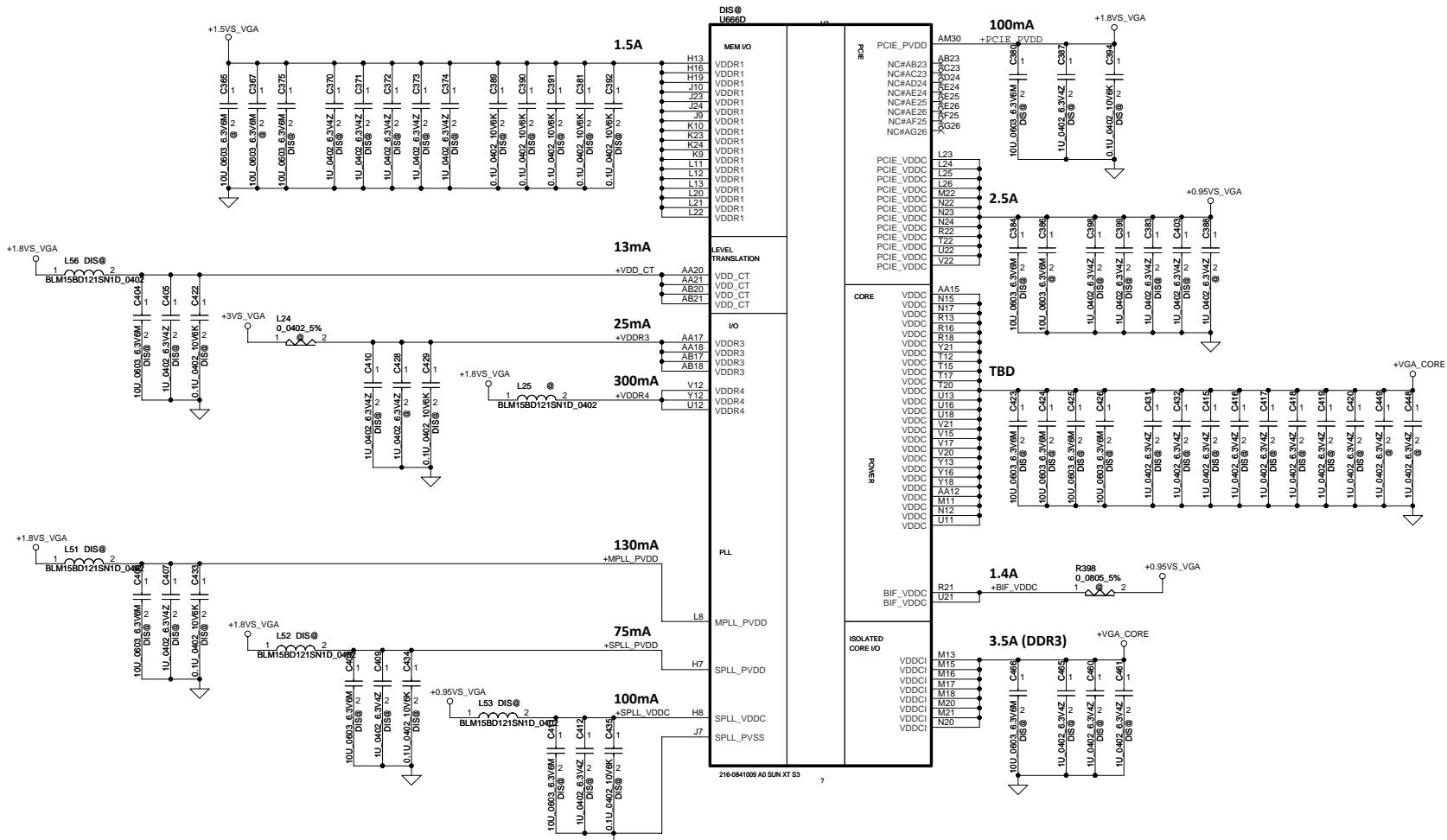
+VGA_CORE	10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)
VDDCI	3.5A	1	3

+0.95VS_VGA	10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)
BIF_VDDC	1.4A	0	0
SPLL_VDDC	100mA	1	1

+1.5VS_VGA	10uF	1uF	0.1uF
VDDR1	1.5A	3	5

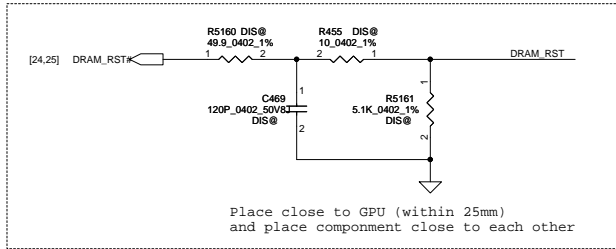
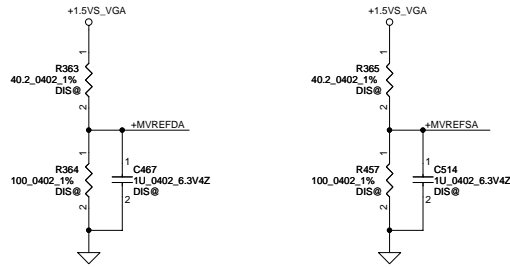
+1.8VS_VGA	10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1
MPLL_PVDD	130mA	1	1
SPLL_PVDD	75mA	1	1
VDDR4	(300mA)	0	0
VDD_CT	13mA	1	1
+TSVDD	13mA	1	1
+DP_VDDR	0	0	0
+DP_VDDC	0	0	0

+3VS_VGA	10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)

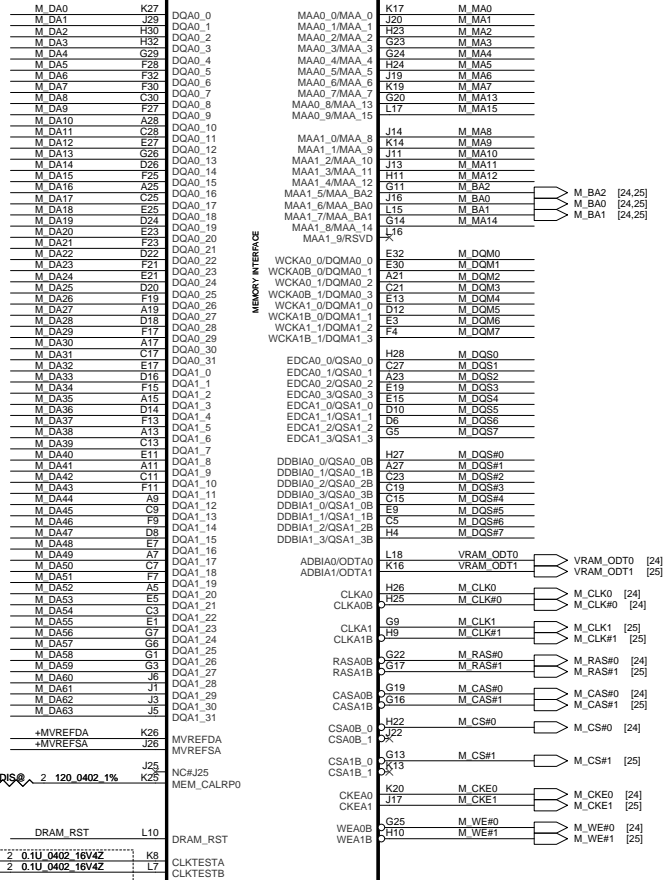


MEM I/F

[24,25] M_DA[63..0] M_DA[63..0]
[24,25] M_MA[15..0] M_MA[15..0]
[24,25] M_DQM[7..0] M_DQM[7..0]
[24,25] M_DQS[7..0] M_DQS[7..0]
[24,25] M_DQS#[7..0] M_DQS#[7..0]

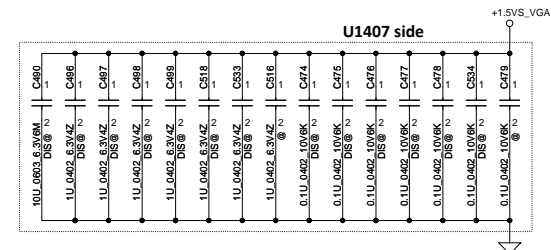
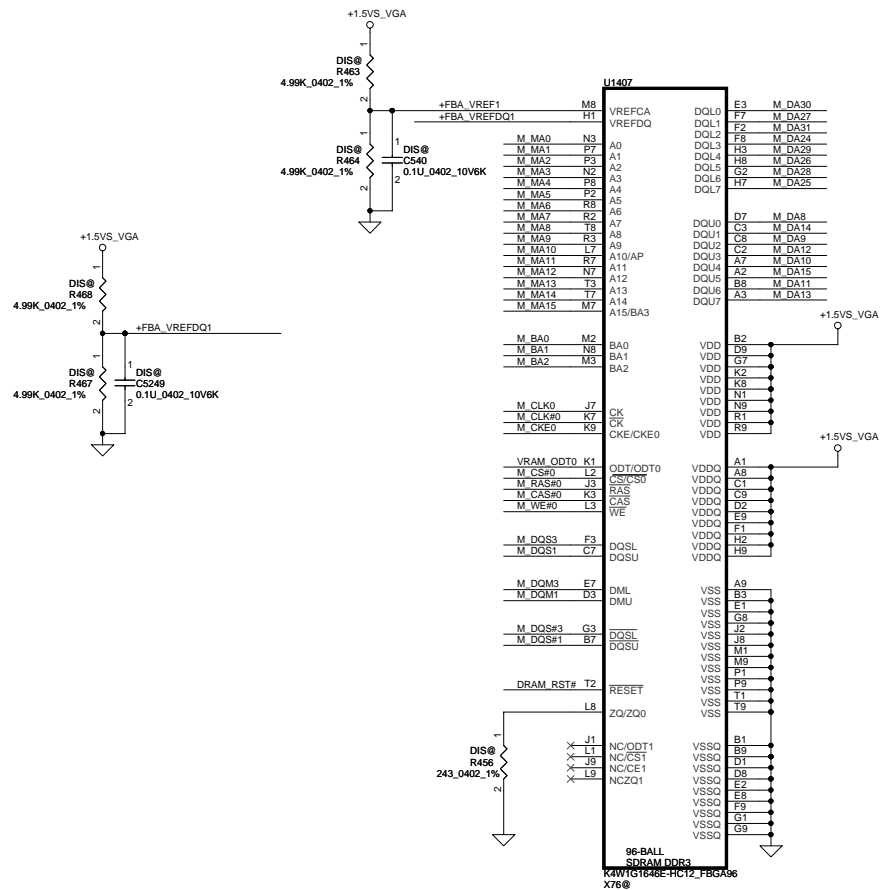
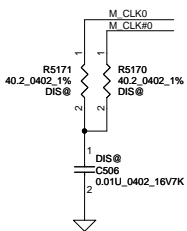
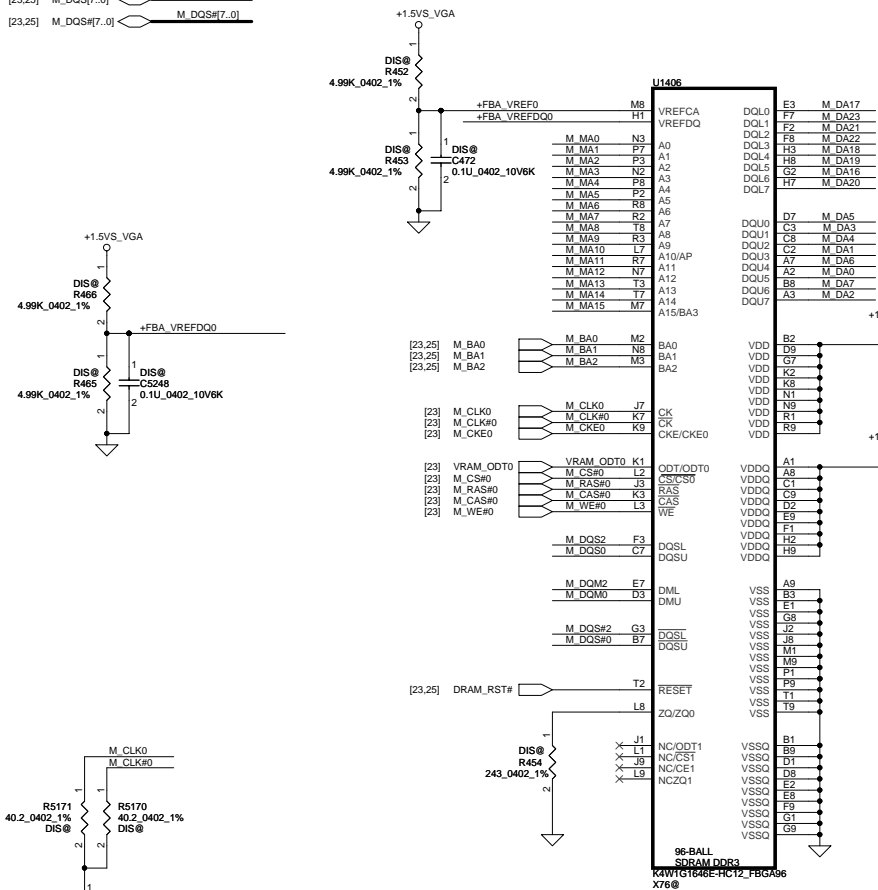
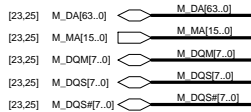


Place close to GPU (within 25mm)
and place component close to each other



Route 50ohms single-ended/100ohm diff and keep short
debug only, for clock observation, if not need, DNI.

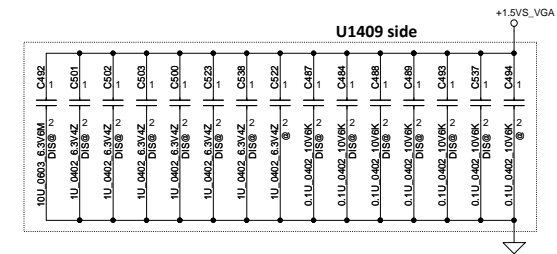
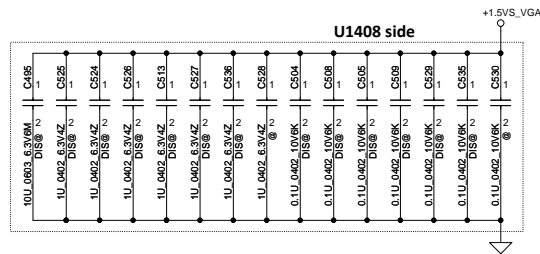
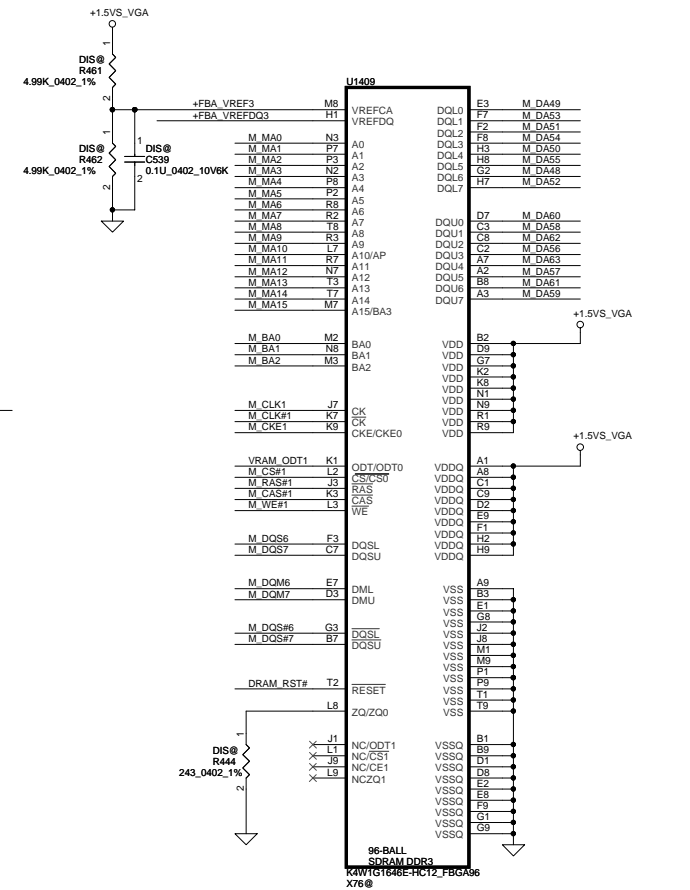
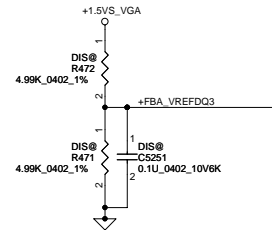
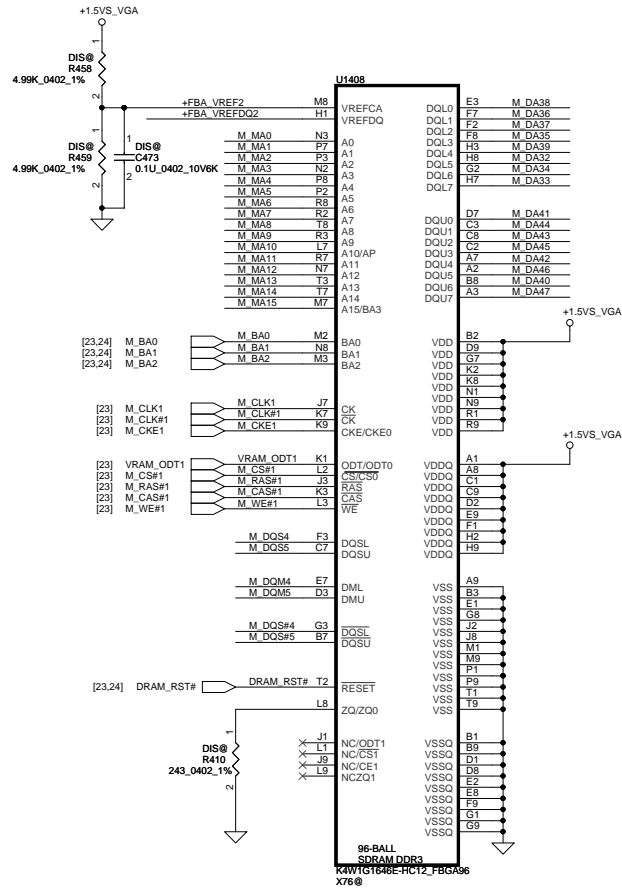
MEM Lower 32-bits



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Issued Date	2013/02/20	Deciphered Date	2012/07/01	Title	SUN VRAM A Lower	
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MEM Upper 32-bits

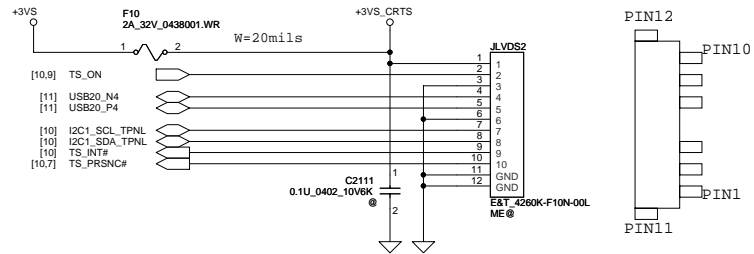
[23,24]	M_DA[63..0]	M_DA[63..0]
[23,24]	M_MA[15..0]	M_MA[15..0]
[23,24]	M_DQM[7..0]	M_DQM[7..0]
[23,24]	M_DQS[7..0]	M_DQS[7..0]
[23,24]	M_DQS# [7..0]	M_DQS# [7..0]



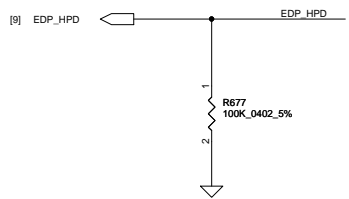
Security Classification	Compal Secret Data			Title	
Issued Date	2013/02/20	Deciphered Date	2012/07/01	SUN VRAM A Upper	
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Touch Screen Conn

P/N:SP01000TF10



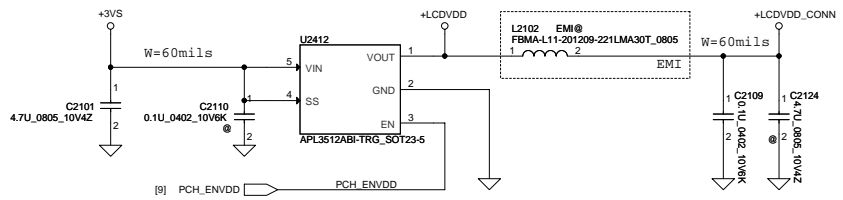
HPD Inversion for eDP



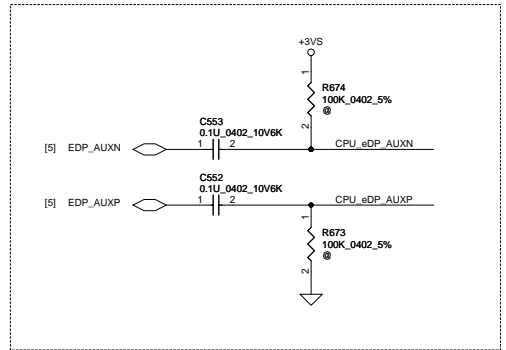
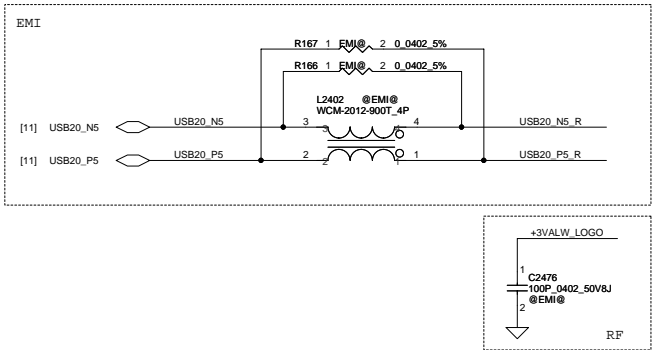
LCD POWER CIRCUIT

SS table

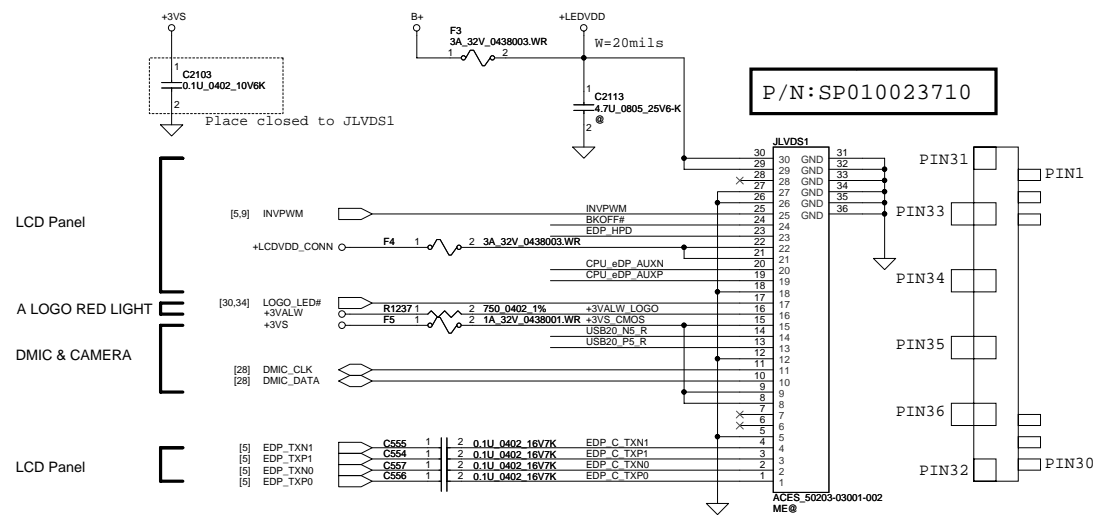
Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS



eDP Panel Conn

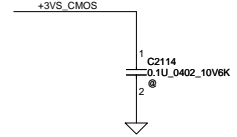


P/N:SP010023710



Camera Modul POWER CIRCUIT

CMOS SUSPEND 2.4mA



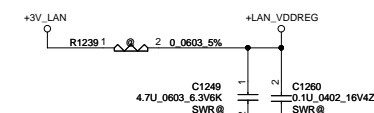
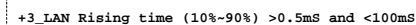
DMIC & CAMERA module pin define

No	SIGNAL
1	VCC (3.3V)
2	D-
3	D+
4	GND_CAM
5	GND_DMIC
6	MIC_C
7	MIC_D
8	MIC_VCC

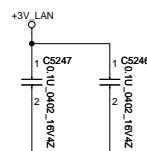
Touch PANEL module pin define

No	I2C	USB
1,2	VCC (3.3V)	VCC (3.3V)
3	Reset	Reset
4	SDA	NC
5	SCL	NC
6	INT	NC
7	NC	D-
8	NC	D+
9,10	GND	GND

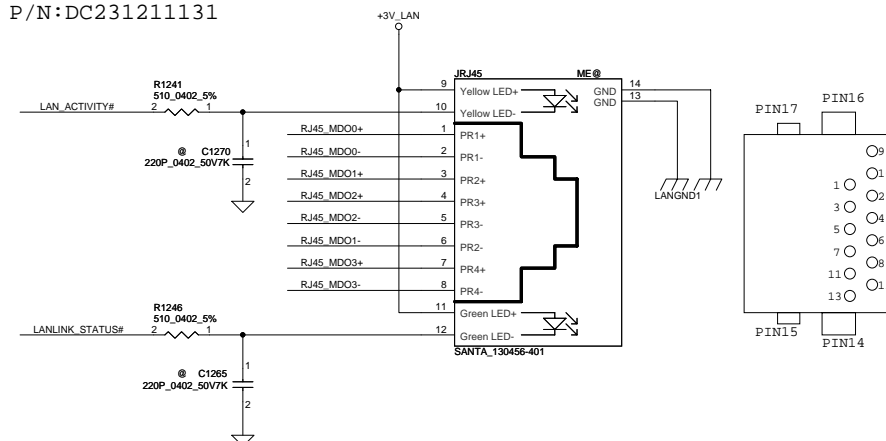
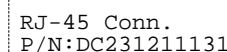
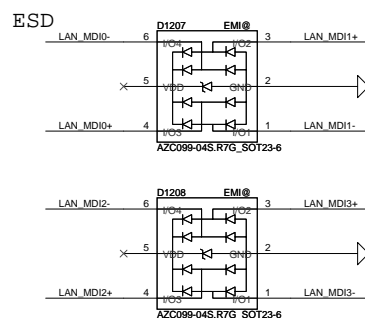
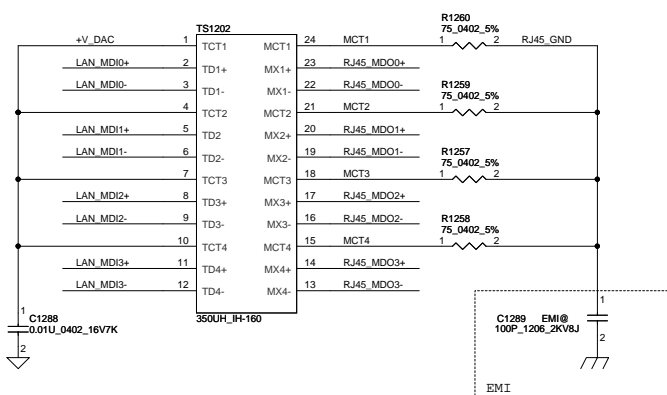
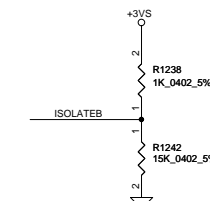
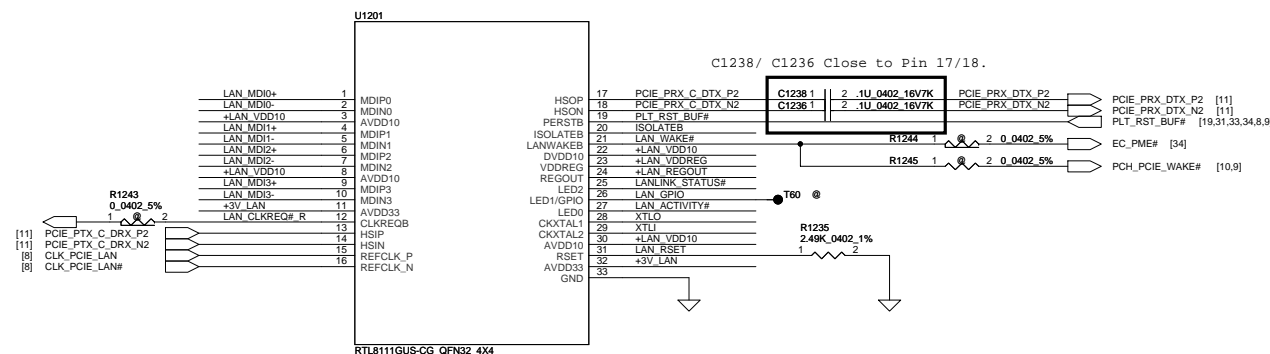
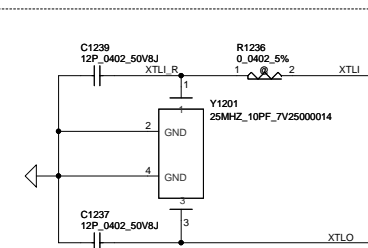
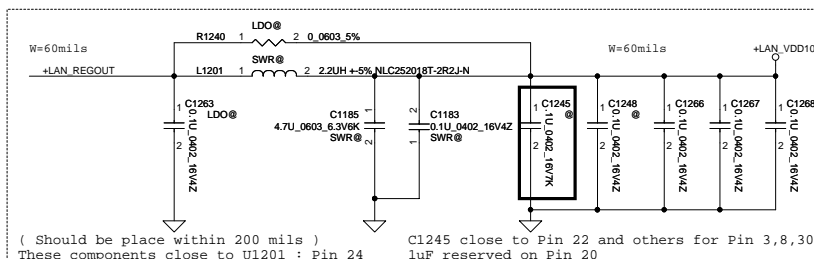
LAN RTL8111GUS



These caps close to U1201 : Pin 23



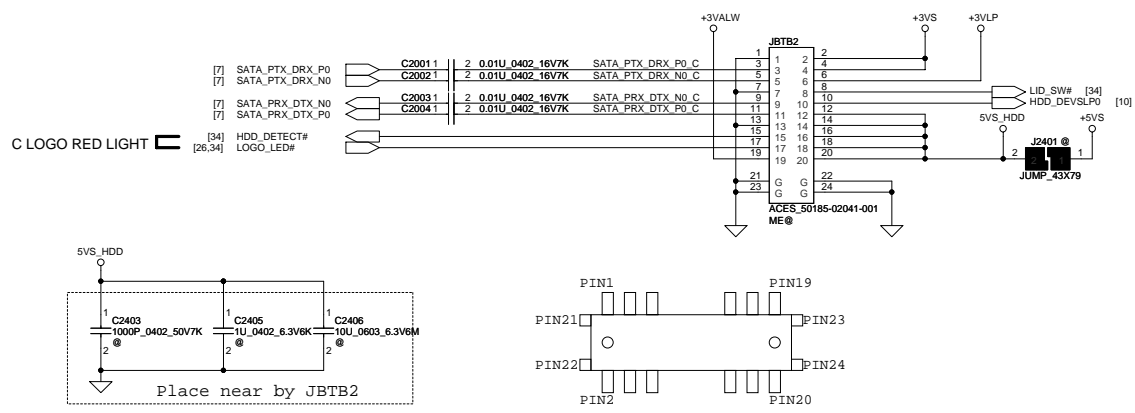
These caps close to U1201 : Pin 11,32



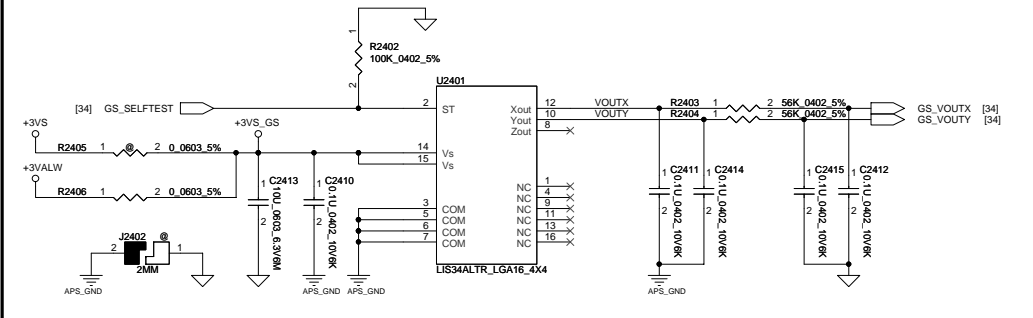
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2013/02/20	Deciphered Date	2012/07/01	Title	LAN RTL8111GS	
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Date:				Friday, February 26, 2014	Sheet	29 of 46

SATA HDD BTB Conn

P/N:SP011208141

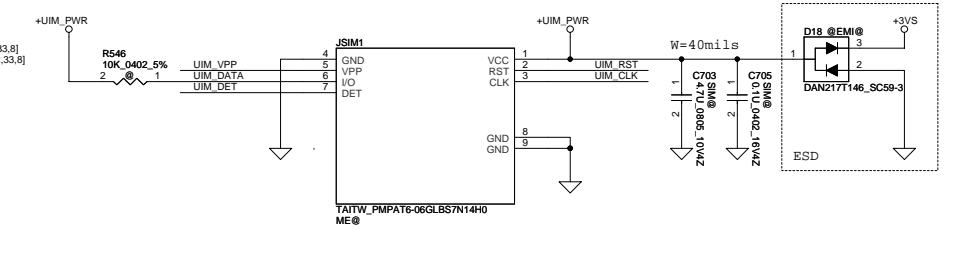
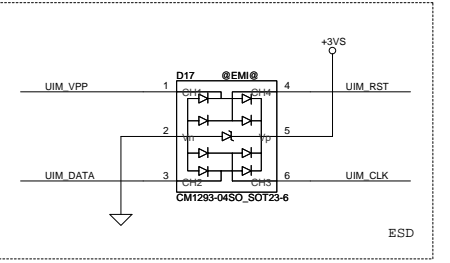
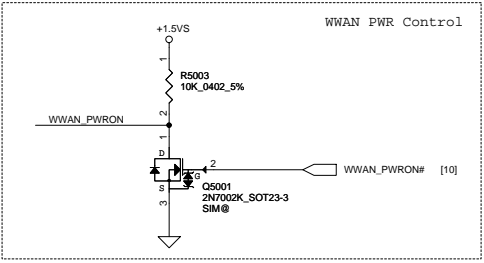
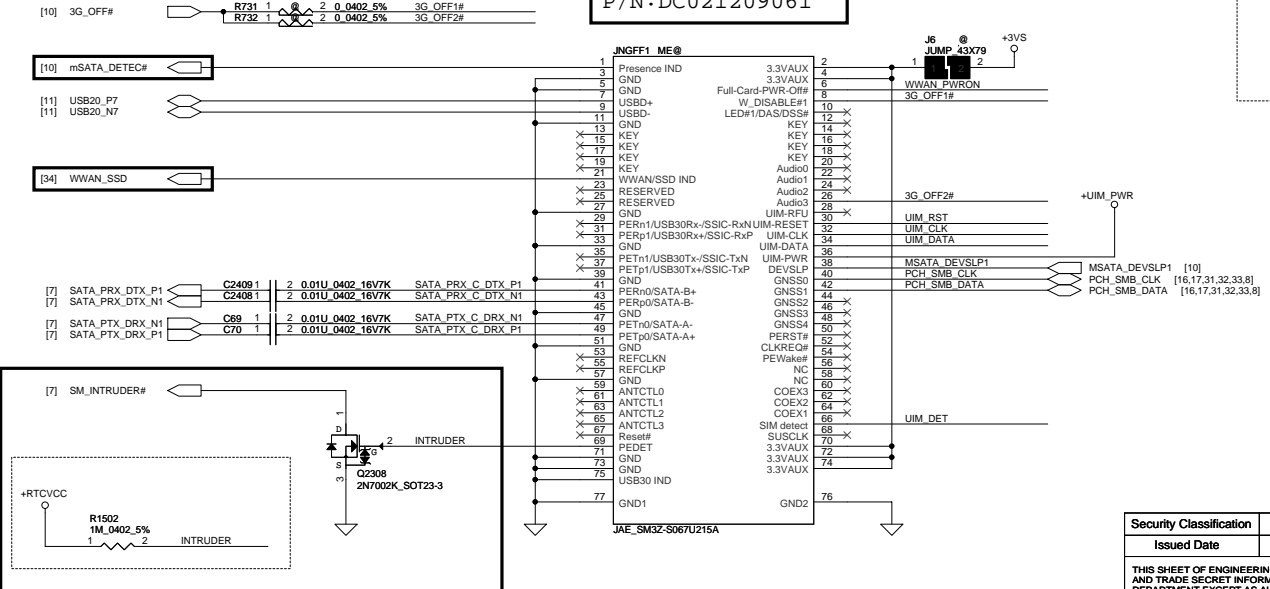


APS G-Sensor



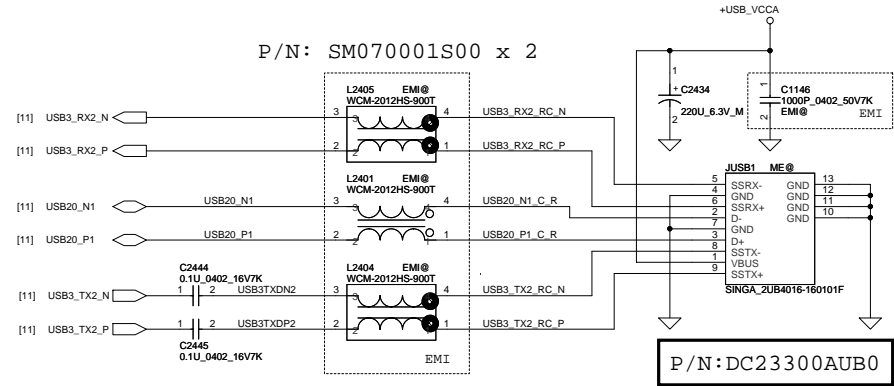
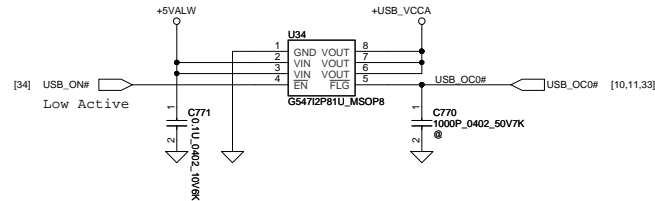
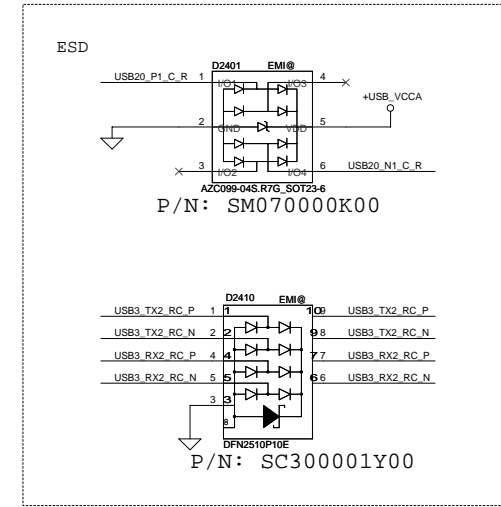
NGFF mSATA/WWAN Conn

P/N:DC021209061

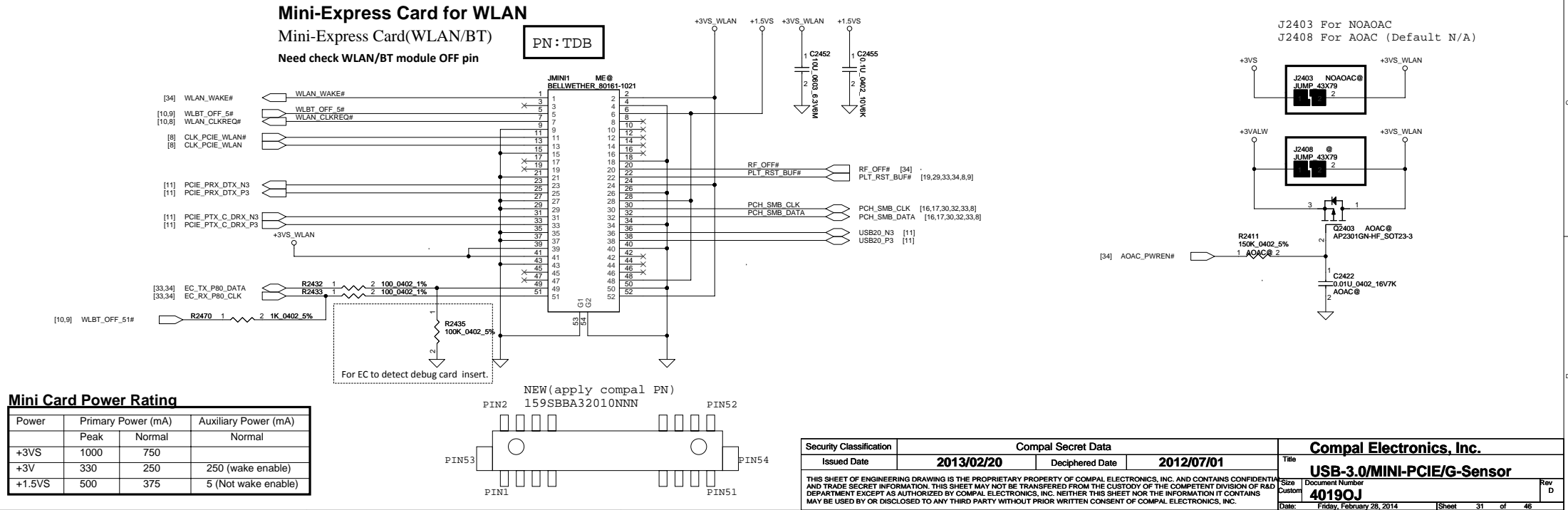


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Size	Custom	Document Number	40190J	Rev	D
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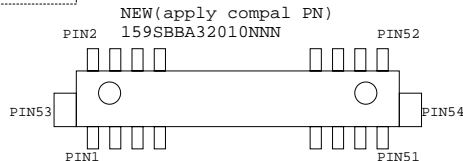
USB30 Conn



WLAN Mini Card

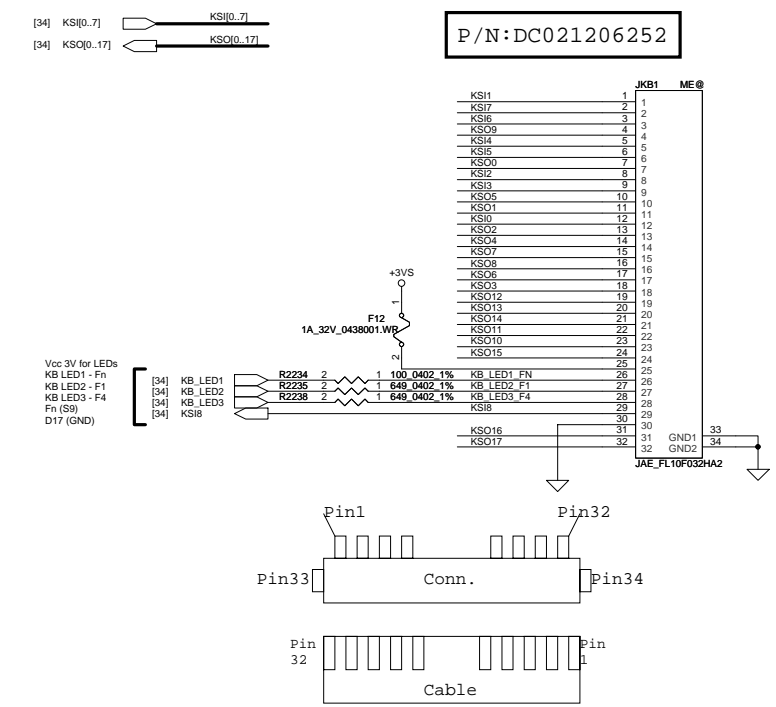


Mini Card Power Rating				
Power	Primary Power (mA)		Auxiliary Power (mA)	
	Peak	Normal	Normal	
+3VS	1000	750		
+3V	330	250	250 (wake enable)	
+1.5VS	500	375	5 (Not wake enable)	

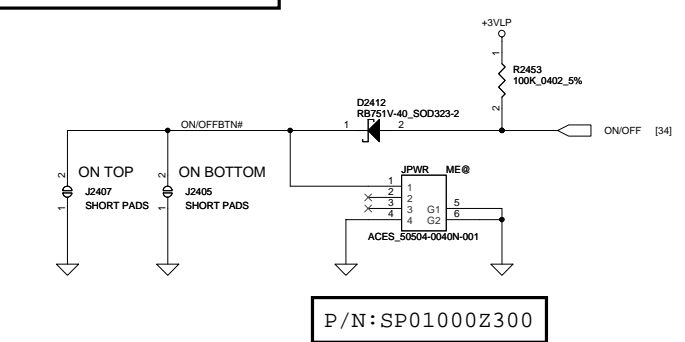


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/02/20	Deciphered Date	2012/07/01	Title	USB-3.0/MINI-PCIE/G-Sensor
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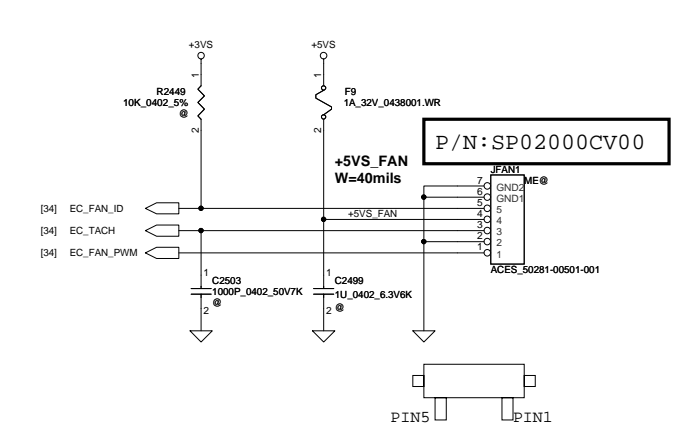
Int KB Conn



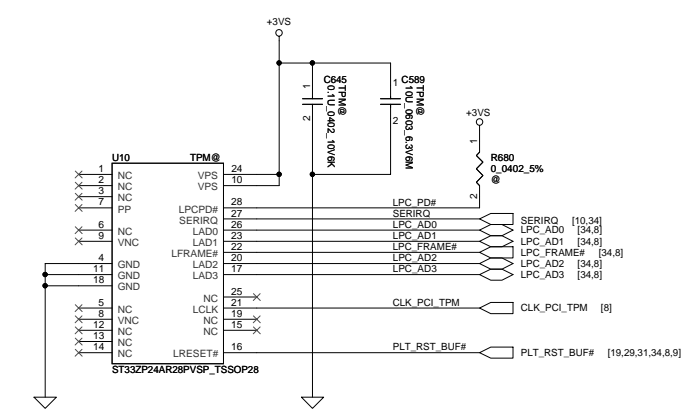
PWRBTN Conn



FAN Conn

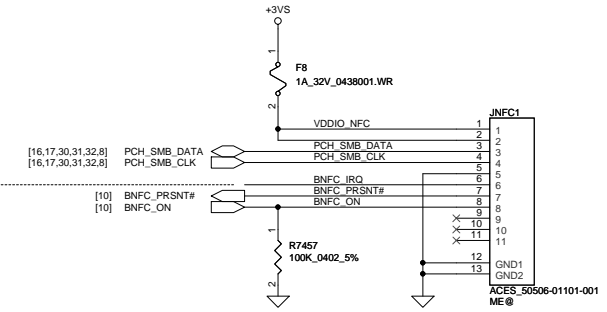
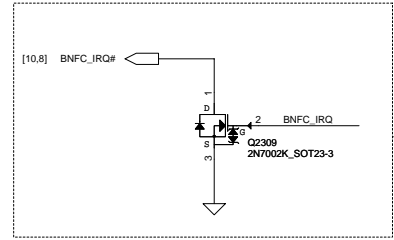


TPM



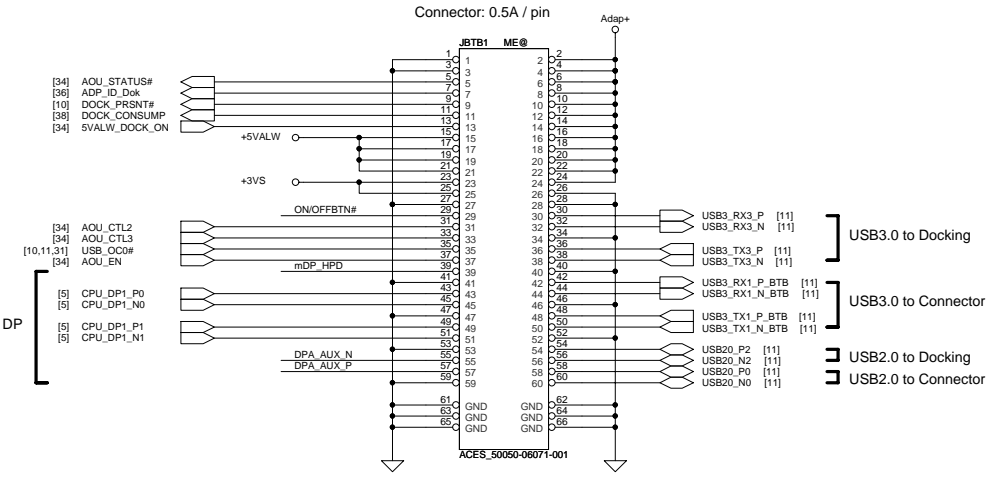
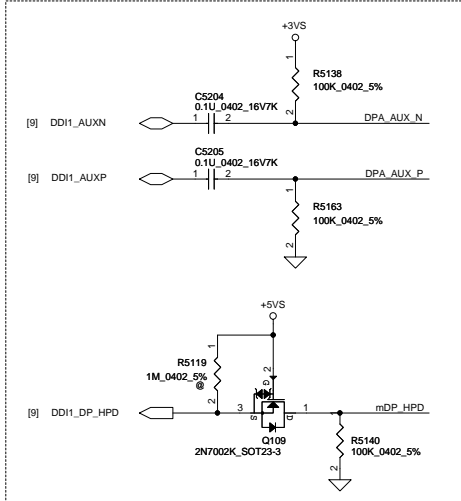
NFC

- Module Pin define
- 1.IP/VBAT
 - 2.IP/VDDIO
 - 3.IO/I2C-SDA
 - 4.I/I2C-SCL
 - 5.G/GND
 - 6.O/IRQ-NFC
 - 7.O/NFC_Presence#
 - 8.I/REG_UP
 - 9.OP/VDD_Ext_SE
 - 10.IP/UIM_PWR
 - 11.IO/SWP

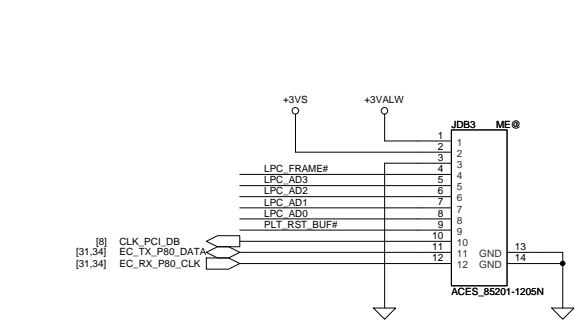


I/O Board Conn

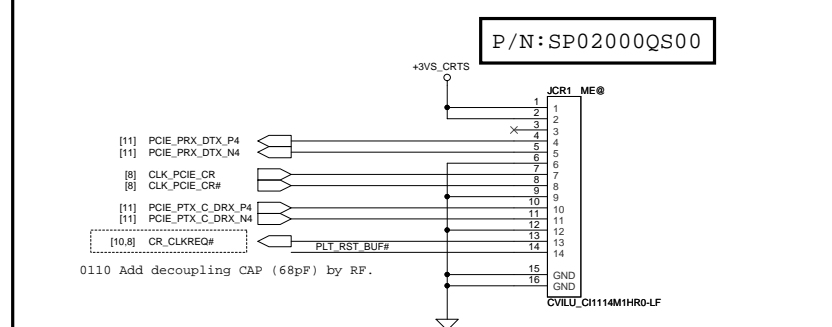
P/N:SP01001BY00



Debug Conn



Card Reader Conn



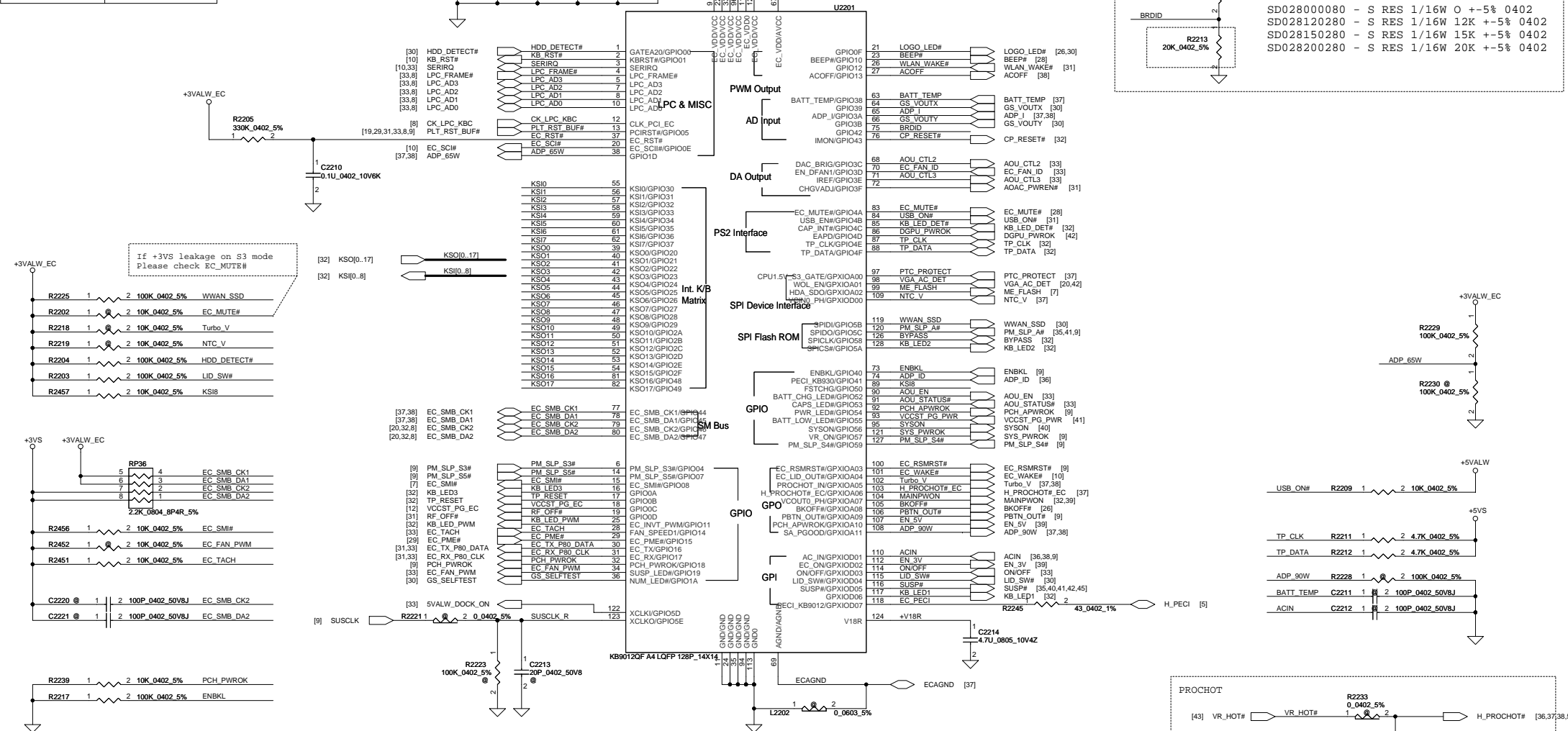
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/02/20	Deciphered Date	2012/07/01	Title	PBTN/FAN/TPM/RTC/I/O Board
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EC KB9012

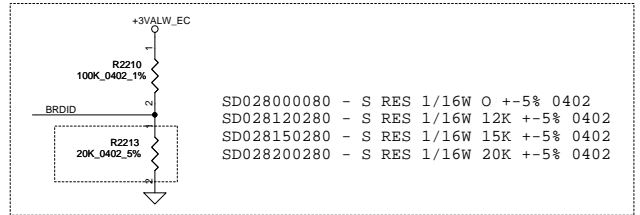
KB9012 A4 v.22

GPIO W/O internal-PH:

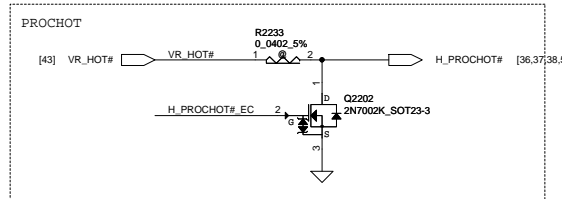
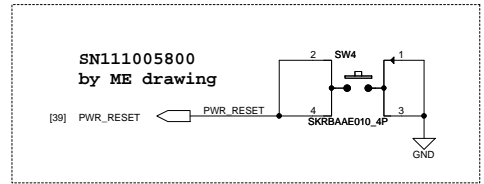
1. GPIO44	6. GPIO4B
2. GPIO45	7. GPIO4E
3. GPIO46	8. GPIO4F
4. GPIO47	9. GPIO50
5. GPIO4A	10. GPIO5B



Vcc	3.3V +/- 5%				
R2210	100K +/- 1%				
Board ID	R2213	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	EC AD
SDV	0K +/- 5%		0.000V	0.300V	0x00 - 0x0B
FVT	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
SIT	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
SVT	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30

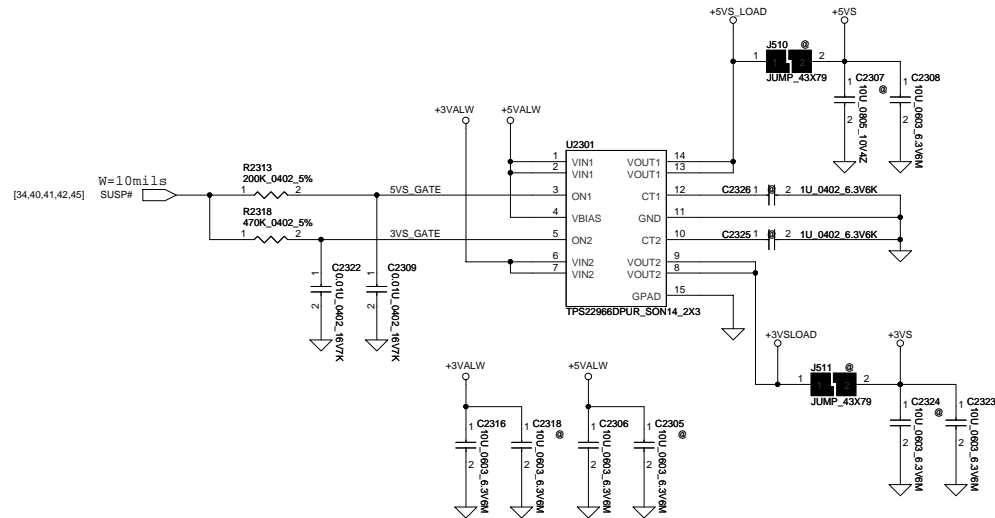


SD028000080	-	S	RES 1/16W 0 +/-5% 0402
SD028120280	-	S	RES 1/16W 12K +/-5% 0402
SD028150280	-	S	RES 1/16W 15K +/-5% 0402
SD028200280	-	S	RES 1/16W 20K +/-5% 0402

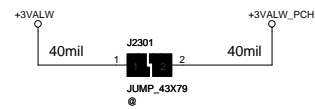


Security Classification	Compal Secret Data	Title	
Issued Date	2013/02/20	Deciphered Date	2012/07/01
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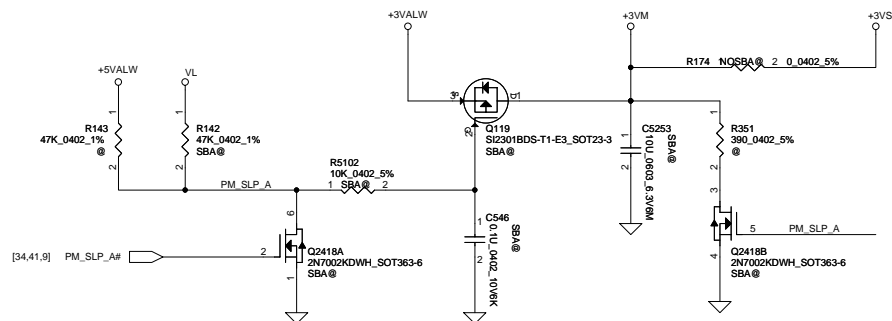
+5VALW TO +5VS
+3VALW TO +3VS



+3VALW TO +3VALW(PCH AUX Power)

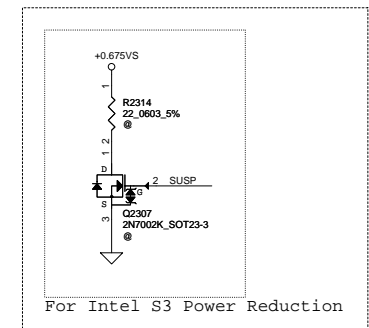
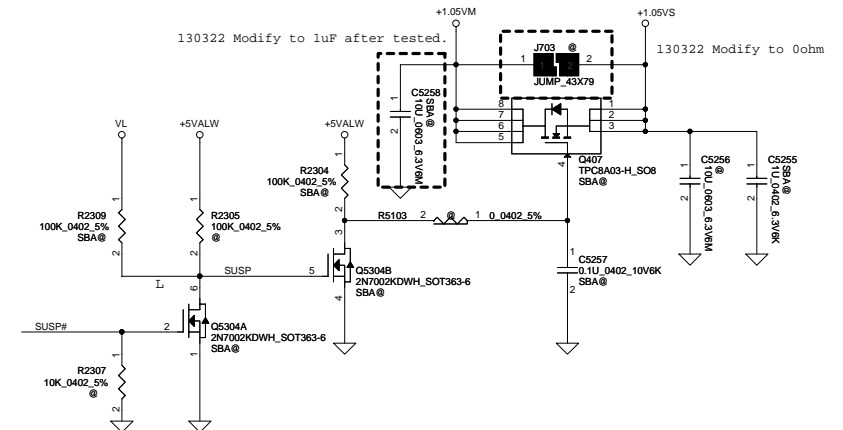


+3VALW TO +3VM (SBA)

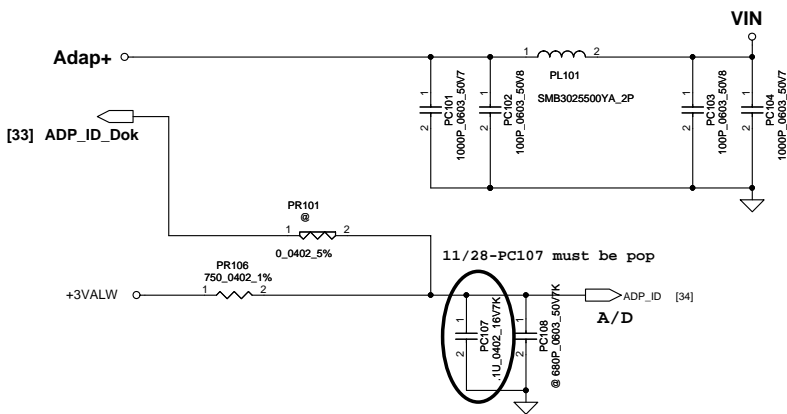


PJ703 Short => NOSBA
PJ703 Open => SBA

$R_{ds(on)}$ $V_{GS}=4.5V$, $I_D=8.5A$, $7m\Omega$ (Max)

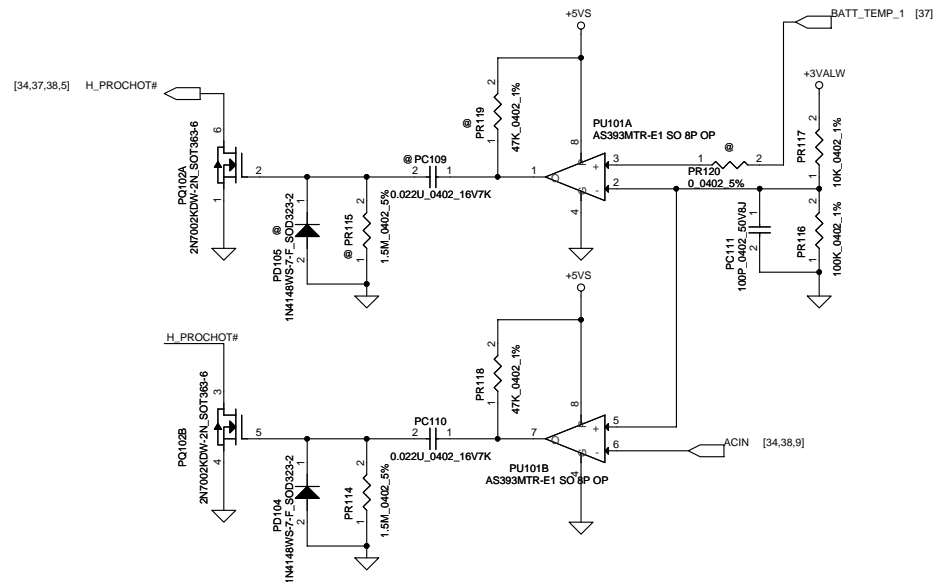
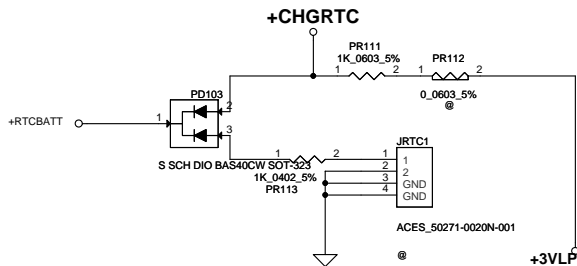


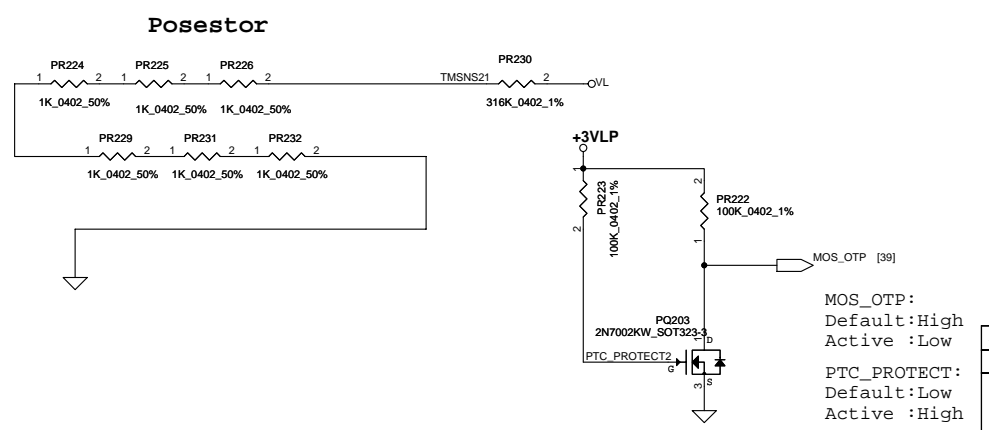
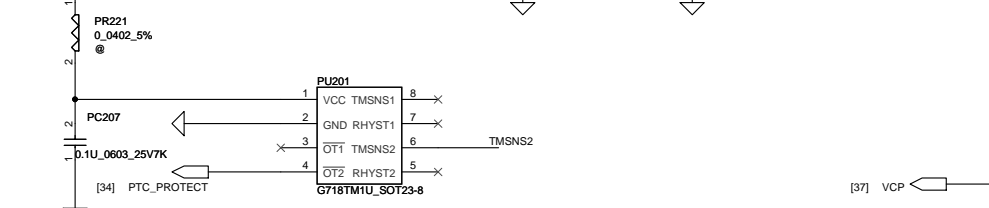
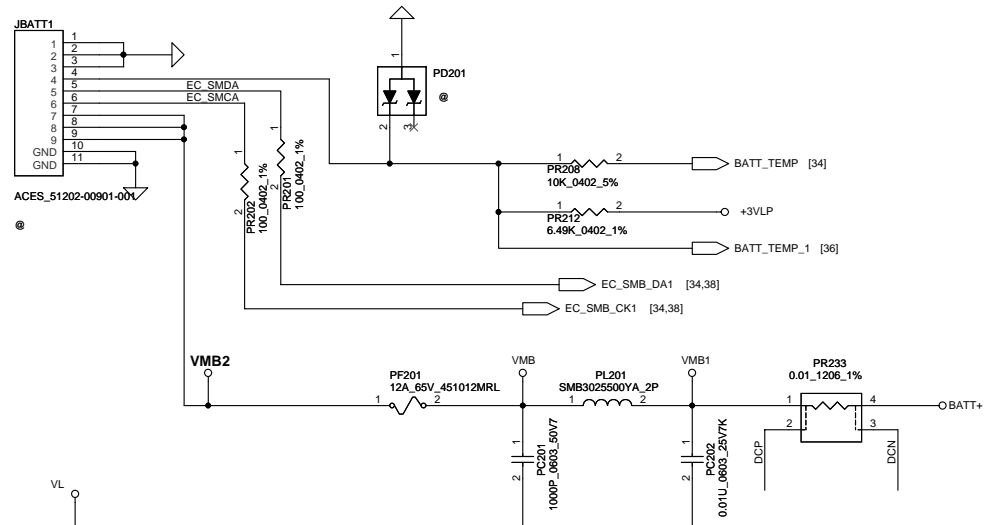
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2013/02/20	Deciphered Date	2012/07/01	Title	DC Interface	
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				Date:	Friday, February 28, 2014	Sheet 35 of 46



ADP_ID

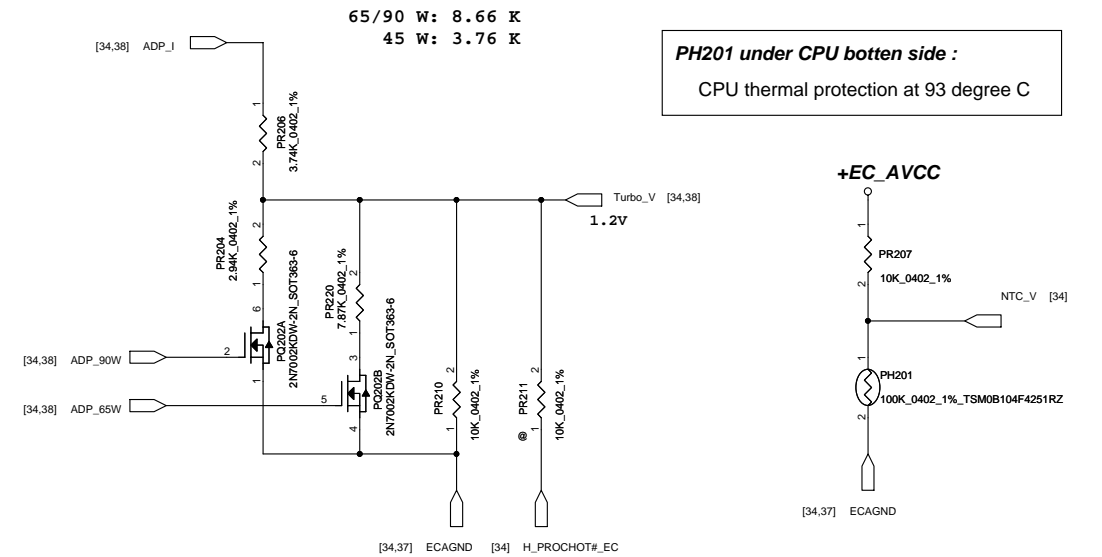
AC Adapter	45W	65W	90W
R(ohm)	118	287	549
ADP_ID(V)	0.449	0.913	1.395
Detection	<=0.663,	<=1.134,	<=1.618
-Voltage(V)	>0.234	>0.693	>1.172





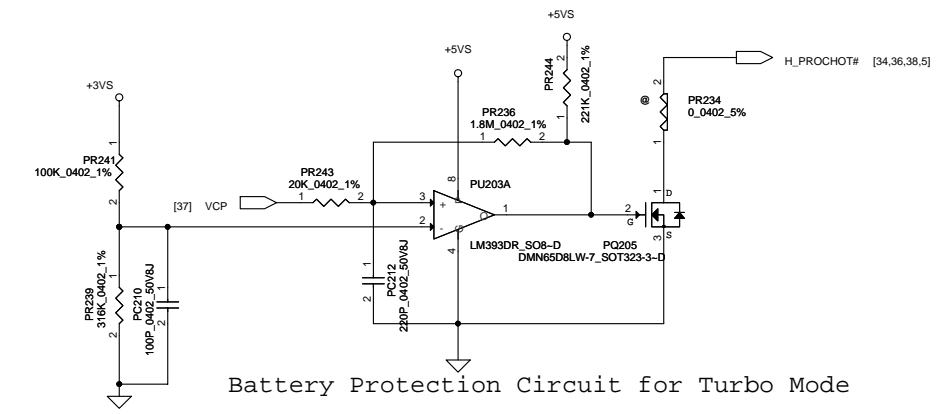
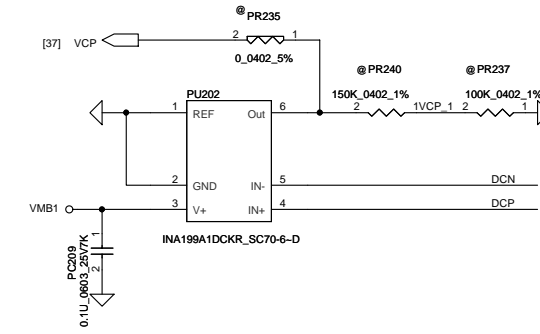
MOS_OTP:
Default:High
Active :Low

PTC_PROTECT:
Default:Low
Active :High



PH201 under CPU botten side :
CPU thermal protection at 93 degree C

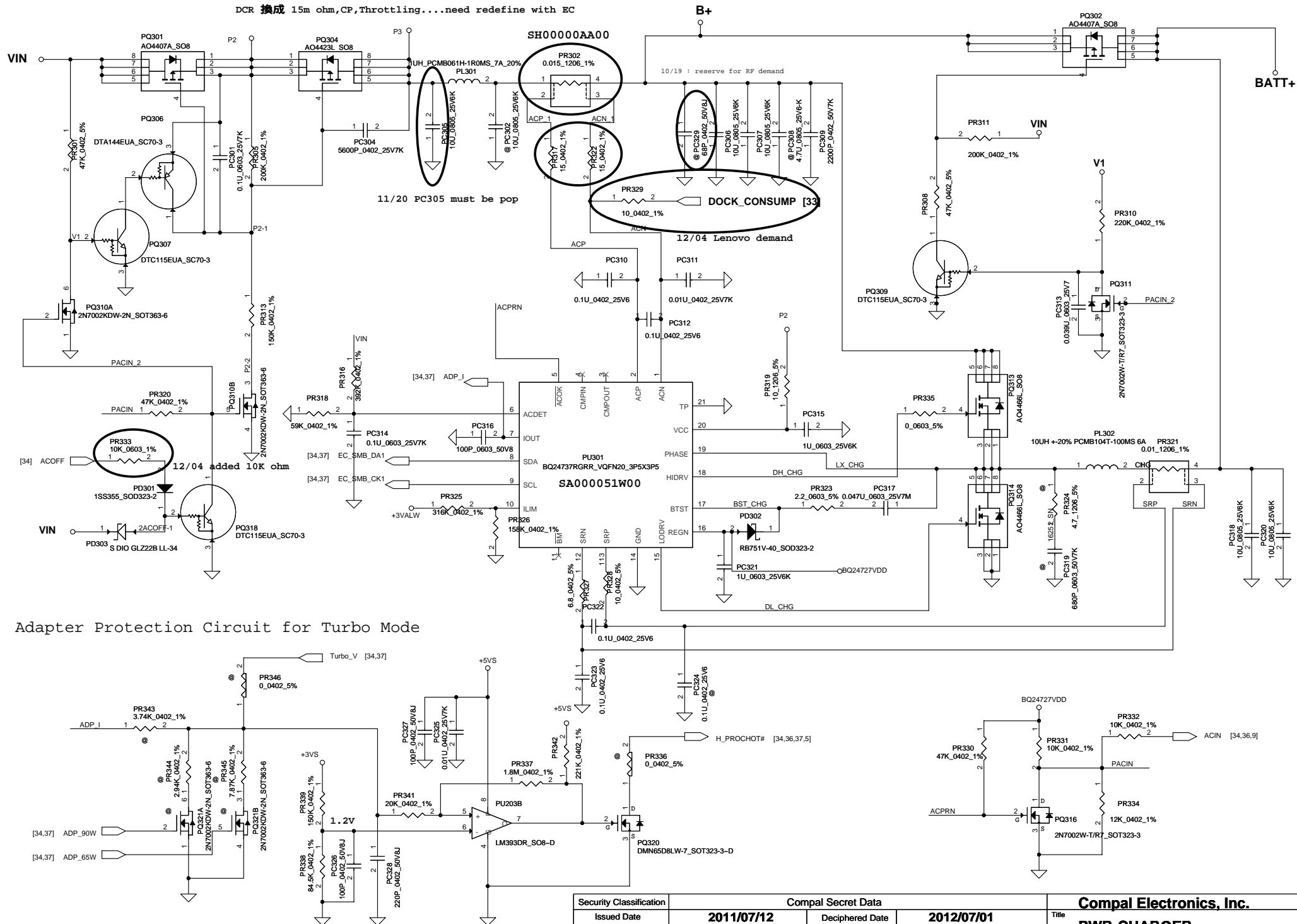
PH201: Temp. Rman. Rnor. Rmin. (Kohm)
93 7.3419 7.0792 6.8253



Battery Protection Circuit for Turbo Mode

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2011/07/12				PWR-BATTERY CONN/OTP			
Deciphered Date				2012/07/01				40190J			
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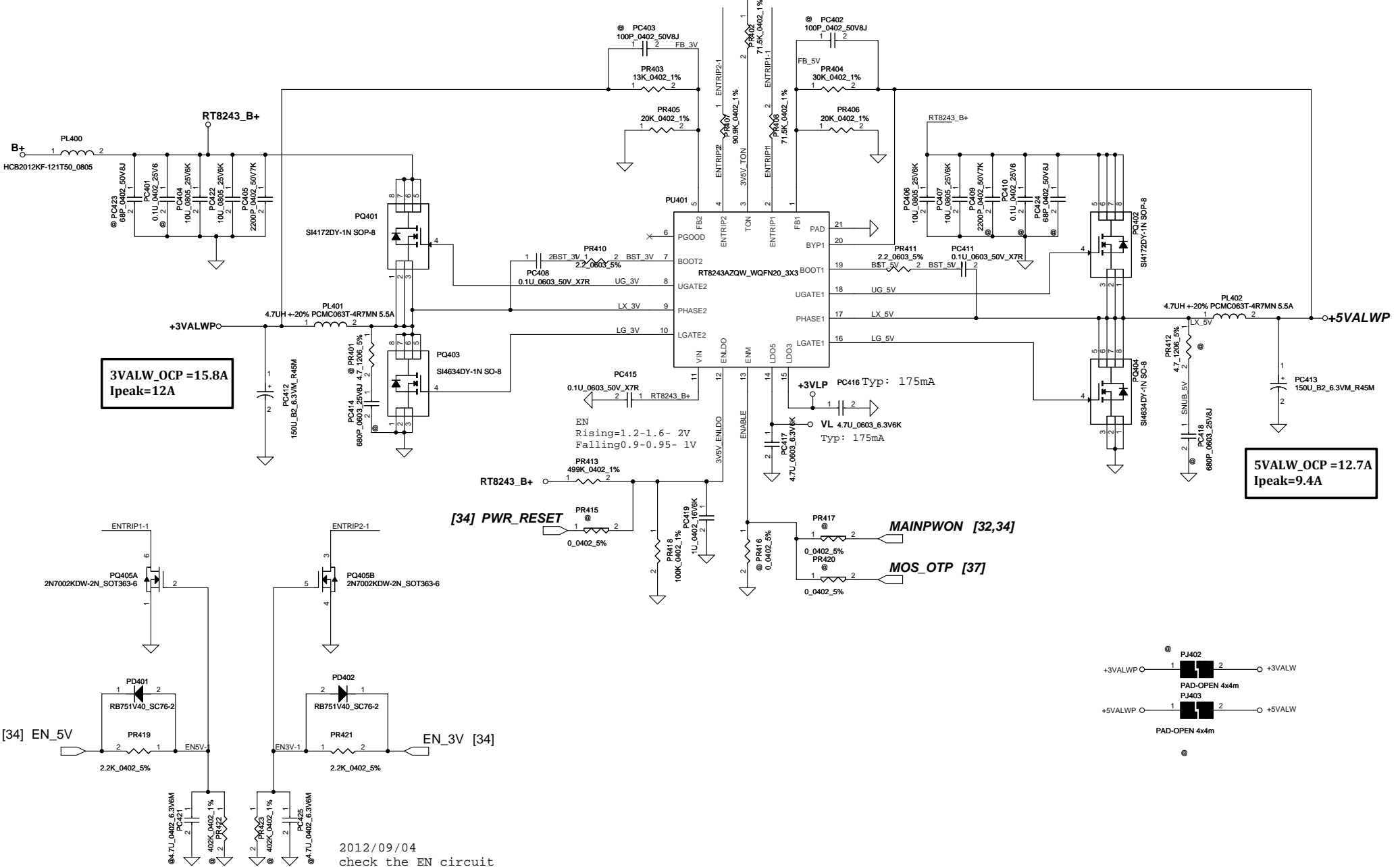
DCR 换成 15m ohm,CP,Throttling....need redefine with EC



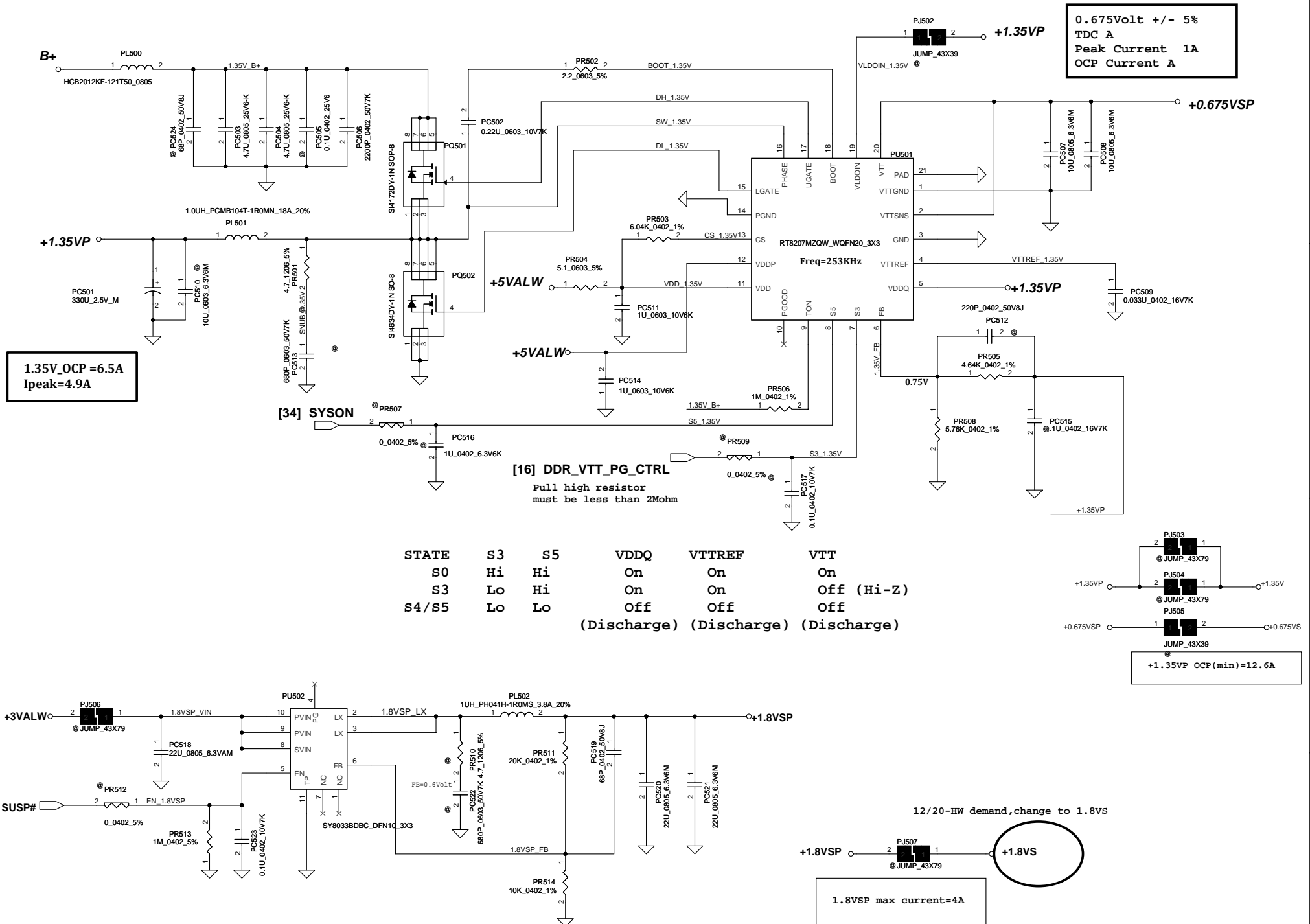
Adapter Protection Circuit for Turbo Mode

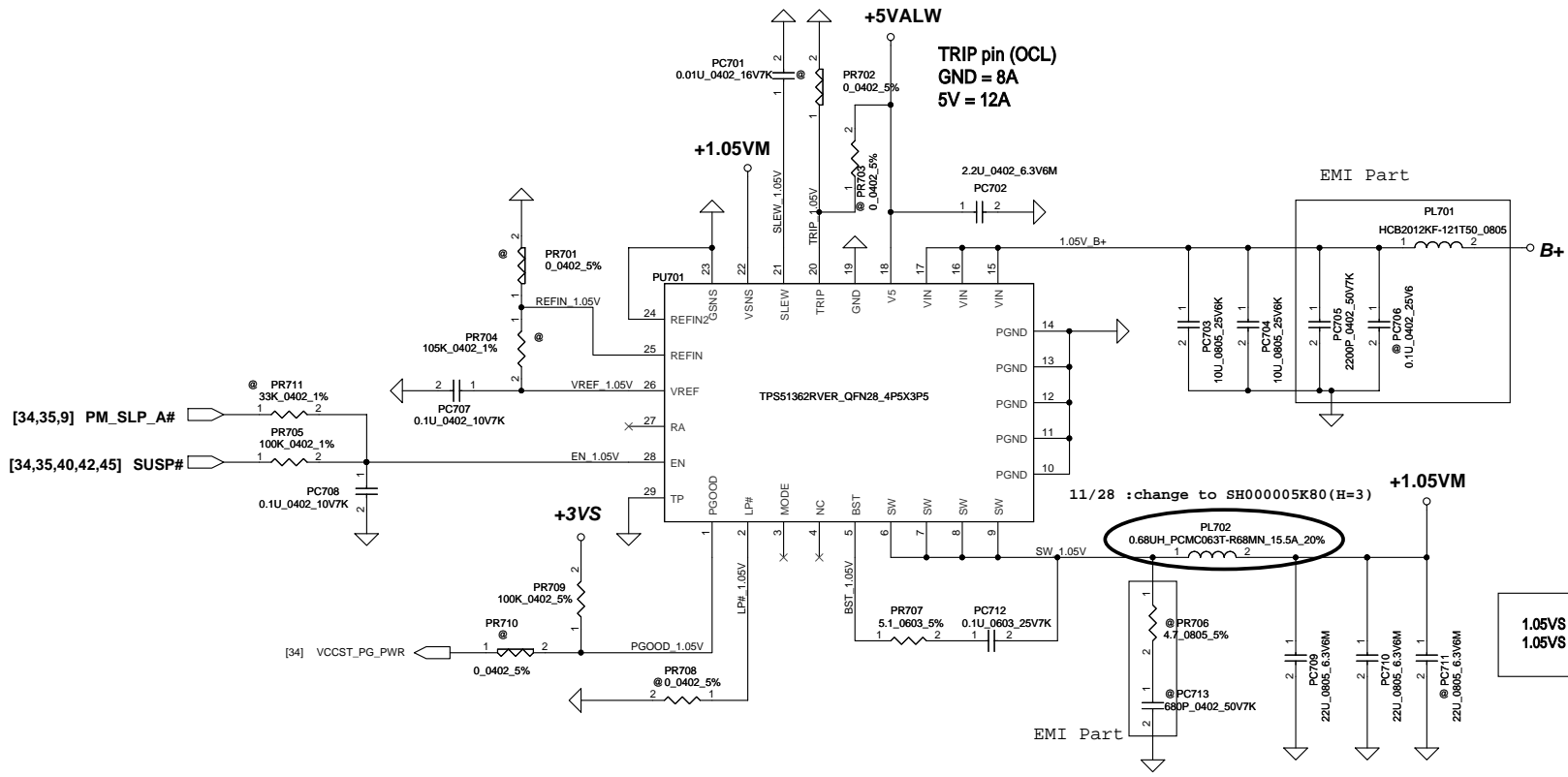
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	PWR-CHARGER
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TON (1)SMPS1=305KHZ (+5VALWP)
(2)SMPS2=357KHZ(+3VALWP)



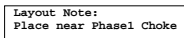
Security Classification		Compal Secret Data		Title	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	PWR-3VALWP/5VALWP	
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1.05VS OCP = 8A (Trip = GND)
1.05VS OCP = 12A (Trip = 5V)

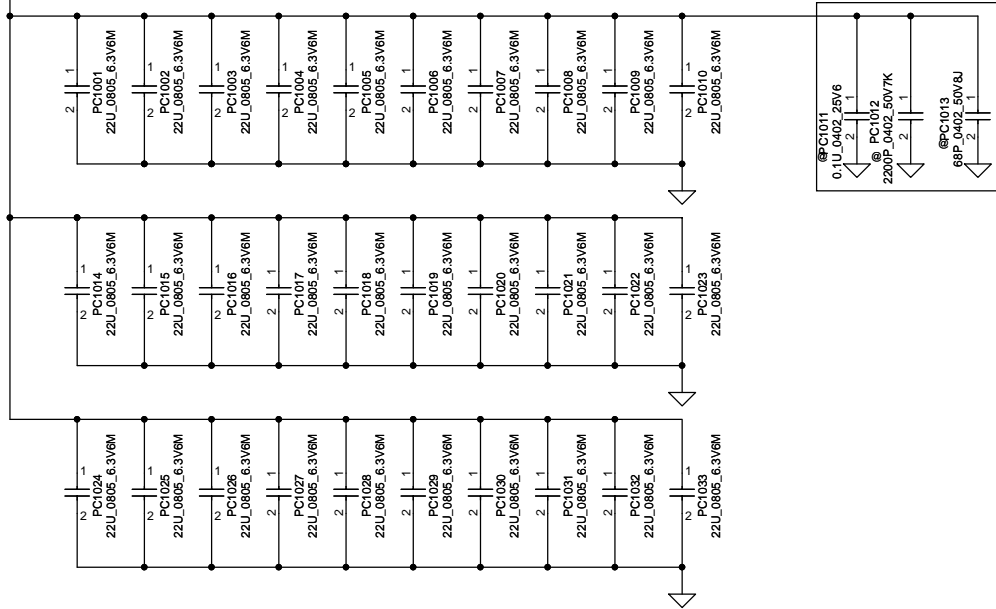
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	PWR-+1.05VM
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Default

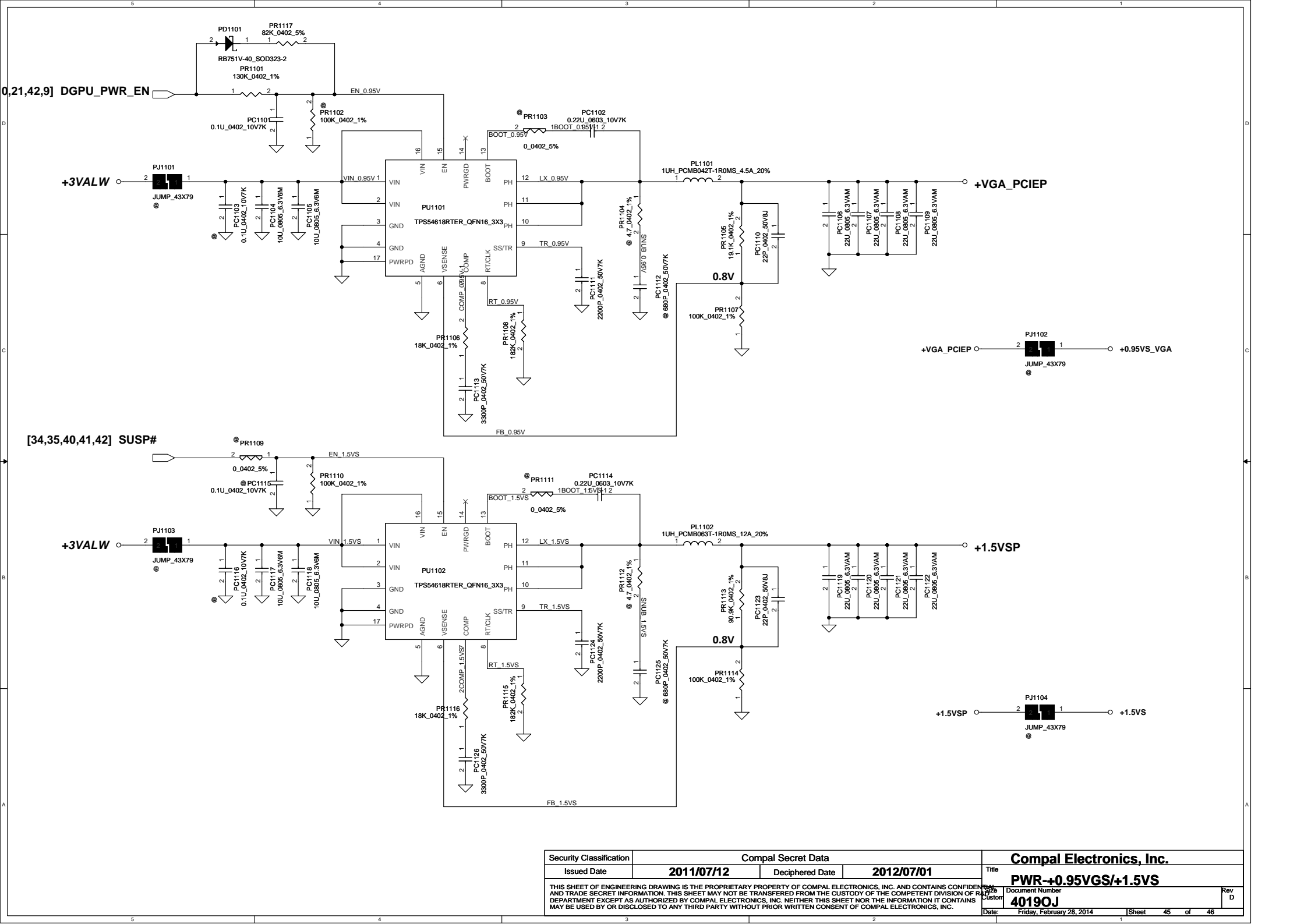
+CPU_CORE

30 X 22u/0805

RF request



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	PWR-PROCESSOR DECOUPLING
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Item	Reason for change	PG#	Modify List	Date	Phase
1	0 ohm change to short pad		PR101, PR221, PR415, PR417, PR420, PR710, PR815, PR832, PR843, PR848, PR859, PR905, PR907, PR908, PR913, PR922, PR112		
2	HW's request, add SBC function.		net name from "PM_SLP_A#" to "M_PWR_ON"		
3	Increase charger current limit.		PR326 changes from 100k to 158k		
4	Shortage on 0.33u capacitor.		PR705 changes to 100k & PC708 changes to 0.1u		
5	HW changes power sequence.	P41	PR711 from 100k to 33k		FVT
6	Disable BATT one shoot circuit	P36	Unpop PR120, PC109, PC115, PR119, PD105	2013/04/25	SIT
7	0 ohm change to short pad	ALL	PR346, PR1103, PR1111, PR234, PR235, PR336, PR701, PR702, PR931, PR507, PR509, PR512, PR1109	2013/04/30	SIT
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	PIR (PWR)
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